An 80 x 25 Pixel CMOS Single-Photon Range Image Sensor with a Flexible On-Chip Time Gating Topology for Solid State 3D Scanning

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***Abstract*— A solid state 3D scanner based on a pulsed laser diode source and narrow time gating of a 2D CMOS single photon avalanche diode (SPAD) detector array is presented. The imager uses an on-chip delay-locked loop to program the time gating of 40 sub-arrays individually. The prototype detector has 80 x 25 pixels with a fill factor of 32 % in the sensor area. The chip has been fabricated in a 0.35 µm high-voltage process and occupies a 5.69 x 5.02 mm^2 area. A 3D range image rate of ~5 frames/second with centimeter level precision is demonstrated to passive targets within a range of ~1 meter and FOV of 36 x 57 degrees.**

Keywords—3D scanner; single-photon avalanche diode (SPAD); time gating; SPAD Array

I. INTRODUCTION

Three dimensional imaging of the environment is important for autonomous driving systems, robotic vision and surveillance applications, for example. A low-price and small 3D-scanner would find use also in human-machine interfaces and gaming applications.

A promising technique to realize a small and robust 3D-scanner is to use the optical time-of-flight (TOF) technique with the electronic focal plane scanning approach. In this technique, a laser diode source illuminates the field of view of a single photon avalanche diode array. When the detector array is located at the focal plane of a positive lens, a 3D range image of the field-of-view of the system can be produced without any rotating mirrors or other moving parts. The distance in TOF systems is measured either directly from the time intervals taken by the photons to travel from the laser transmitter to the target and back to the receiver or indirectly by utilizing a phase comparison technique with a continuous wave (CW) modulated source.

With the phase comparison technique, a measurement range of 0.8 – 4.2 m with fairly good accuracy of < 1 % has been achieved [1]. However, the measurement range achieved with this technique is typically short. Another typical realization utilizes a pulsed laser source, which allows for high single shot precision and in many cases also wider measurement range, even km´s with high enough transmitter energy and single photon detection mode [2].

The pulsed TOF range finding method usually uses the direct distance measurement technique with a time-to-digital or time-to-amplitude converter and can achieve a millimeter level accuracy even to a range of more than a few tens of meters [3]. The drawback of this technique is the sensitivity to background light if the sensor is open for photons during a time window covering the whole measurement range (e.g. 100 ns for a measurement range of 15 m). With strong ambient light conditions, one solution is to use a fast electric shutter to control the sensor's sensitivity to photons by limiting the time interval during which the detectors are enabled for the photon detection [2 – 5]. In this work, the width of the time gating with an electric shutter is set to the minimum and thus the imager is very tolerant to background light.

The fill factor of the sensor array should be high in the focal plane approach to maximize the photon detection efficiency. The larger the SPAD array, the more difficult it is to get a high fill factor due to the large number of routing signals or due to in-pixel electronics. Typically, large arrays with more than 1000 pixels tend to have a small, less than 10 % fill factor [4].

In this work, we propose a CMOS SPAD imager topology utilizing narrow and flexible time gating of a 80 × 25 pixel SPAD array, and show also the first 3D range image measurement results achieved with this device. Although time gating has been successfully implemented in single photon detector arrays before [5], this kind of a programmable and separable time gating of pixel sub-arrays together with the use of a laser diode transmitter with high energy (~1 nJ) sub-ns pulses is suggested here for the first time for 3D range imaging, to the best knowledge of the authors. The flexibility of the time gating is a remarkable advantage since it enables the sub-arrays of the sensor area to be individually set to measure (or scan) different distance windows. The use of sub-ns laser pulses (~100 ps FWHM) allows for a good single shot resolution at the level of 1 – 2 cm.

In the following, the operating principle of the proposed 3D imager is described first. Then the pixel design and architecture of the chip are described. At the end of the

paper, the first 3D range image measurement results are shown.

II. 3D Range Imager Operating Principle

The 3D range imager proposed here is based on the pulsed TOF technique and flexible time gating of the SPADs in the detector array. The detector chip collects binary type 2D cross-sectional images from predetermined distances which are defined by the time gating electronics, see Fig. 1. The chosen measurement range is scanned, and the 3D image is accumulated from the 2D cross-sectional images of the surface of the target resulting from the single shot measurements.

The principle of setting the time gates of sub-arrays at different time (range) locations is shown in Fig. 2. In the prototype circuit, the pixel array is divided into 40 sub-arrays, each of which has 10 × 5 SPADs. The position of the time gates can be programmed individually for each sub-array within the total time window of 24 ns, which corresponds to a range of ~3.6 m. The width of the time gates can be set larger when searching for a target and decrease to the minimum when the target is found and the highest resolution is needed. The partitioning of the large sensor array into sub-arrays increases the total 3D frame rate of the system since partial scans around the surface of the target or even multiple targets at different distances can now be implemented without the need to scan over the whole image space and depth.

With a pulsed laser source that has high energy (> 1 nJ) and narrow full width at half maximum (FWHM ~ 100 ps), a single-shot depth resolution of < 2 cm is achievable [6]. The detector time measurement precision depends on the SPAD timing jitter (50 – 100 ps typically) and on the time gating precision. The shifting of the time gate position with respect to each other can be done on-chip in a grid of ~ 100 ps (LSB) in the prototype. The length and position of the time gates are selected from altogether 240 outputs of two on-chip delay-locked loops. The selection of the time gate for each sub-array is controlled by the FPGA.

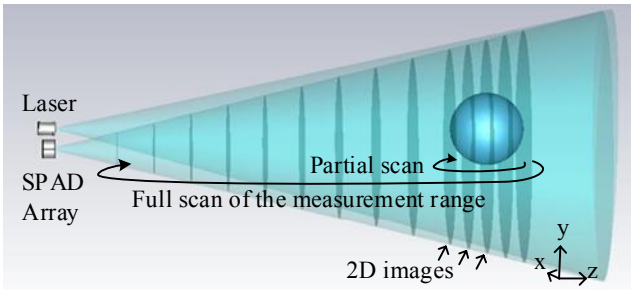

Fig. 1. 3D imaging with cross-sectional 2D images.

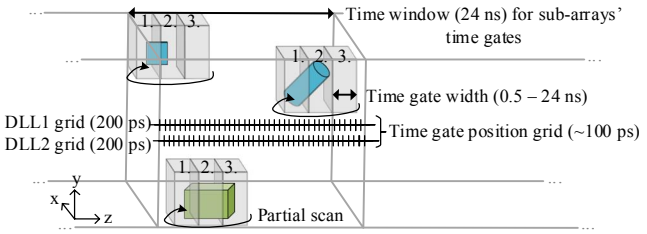

Fig. 2. The 2D pixel array is divided in to 2D sub-arrays whose time gating can be programmed individually.

The laser driver is controlled from the detector chip. In this way the measurement range can be set to begin right at the lens of the detector.

III. Pixel Electronics

In order to get a high fill factor for the sensor part of the chip, the electronics inside the sensor array have been minimized. Biasing switches, 1-bit data storage, and buffering of signals were implemented inside each pixel. A simplified schematic of the pixel is presented in Fig. 3.

At the beginning of the operation, the SPAD is quenched by biasing the anode node of the diode to the voltage supply of 3.3 V. The cathode of the diode is connected to a high-voltage supply of ~22 V. When the quenching switch is turned off, the anode node can be shunted to the ground. This forms the leading edge of the time gate and exposure of the sensor for photons.

The timing diagram of the pixel electronics is presented in Fig. 4. The *load* signal for enabling the SPAD is produced locally at each pixel from the rising edges of *load start* and *load stop* signals coming from outside the sensor array. By transferring signal information in rising edges makes it easier to produce fast and narrow loading pulses to the other side of the large array. In this case, for example, the longest trace lengths are over 2.5 mm. The trailing edge of the time gate is produced by the leading edge of *sample* signal which samples the state of the SPAD into the 1-bit memory cell. After the states of all the SPADs in the array have been sampled, the flip-flops are connected in series and the measurement data is read out from the pixels in series mode.

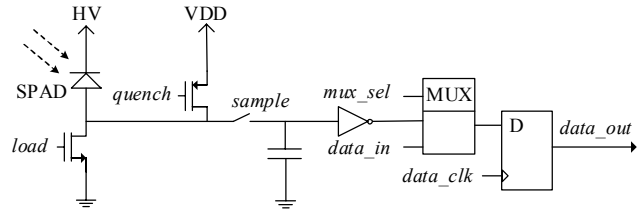

Fig. 3. Schematic of the pixel electronics.

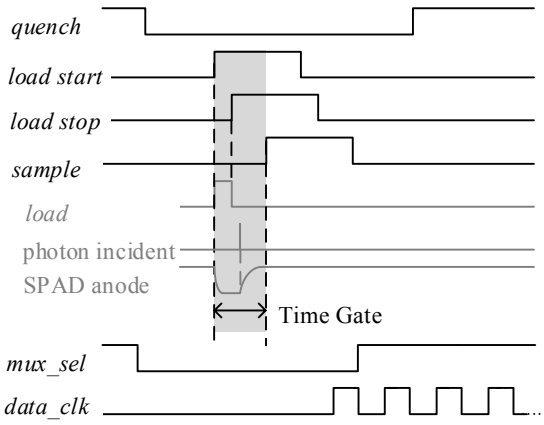

Fig. 4. Timing diagram of pixel electronics.

The size of one pixel is 50 µm × 100 µm and the active area of one SPAD in a pixel is 36 µm × 44 µm. This results in an average fill factor of ~32 % for the whole sensor area. A relatively large SPAD pixel area was chosen to get a high fill factor. The resulting higher noise (DCR) due to the larger SPAD area is not an issue due to the narrow time gates used. The multiplication region of the avalanche diode is produced by a deep nwell/p+ junction and the active area is surrounded by pwell guard rings as in [7]. The SPADs are placed in rows of 80 pixels which all share the same deep nwell. Also, every other of the 25 rows is flipped in the y-direction and placed in the same deep nwell to increase the fill factor.

IV. Detector Architecture

The detector prototype consists of a detector array of 80 × 25 pixels and programmable on-chip time gating, control and data processing with an FPGA, see Fig. 5.

The time gating signals are produced on-chip from two delay-locked loops (DLLs) each of which has 120 outputs. The length of both DLLs is 24 ns with an 83.3 MHz clock signal from the FPGA.

The independent time gating signals for each of the 40 sub-arrays can be selected from the DLL outputs with multiplexers. Hence, time gates at each sub-array can vary with the maximum of ~24 ns in relation to each other. In the prototype, each of the time gates are produced from three independently selectable signals. The selection of the signals is made with 240-to-1 multiplexers (MUX) from the DLLs' 240 outputs. Each of these 3*40 MUXs is controlled by the external FPGA with 8 bits.

In order to be able to place the time window of 24 ns (see Fig. 2) to the desired time position, a control block was implemented. This control block enables the DLLs' output buffers for a specific time window. The control block has a 6-bit counter which counts total DLL cycles after the laser command has been sent. The control block is controlled by the FPGA with 6 bits and enables a time window of 24 ns for the time gating even with a ~1.5 µs delay from the laser pulse.

To be able to measure distances from zero distance, a selectable delay for the laser shoot command has been implemented. The selection is done from one of the 120 DLL outputs with the delay grid of 200 ps. The signal for laser driver circuitry is buffered in the same way as the time gate signals to reduce the effect of temperature and supply voltage changes.

The state of the 2000 SPADs at the trailing edge of the time gate is sampled into in-pixel memory cells. The result is then read out by connecting 80 of these 1-bit registers serially and buffering all the 80 x 25 bits to an external FPGA for further processing. With a 100 MHz readout clock, up to 1 MHz frame rate for single measurement shots can be achieved. The transfer of all of the data to the external FPGA makes the signal processing flexible especially for a prototype version, but at the cost of larger power consumption due to the need of multiple large high speed buffers.

The prototype of the detector chip was fabricated in a cost-effective 0.35 µm high-voltage process and the dimensions of the chip are 5.02 mm × 5.69 mm. The picture of the chip and the layout of one sub-array of pixels are presented in Fig. 6. The layout of the chip is designed so that the array size can be multiplied by two or even four by pipelining the registers and rearranging the power supply pins.

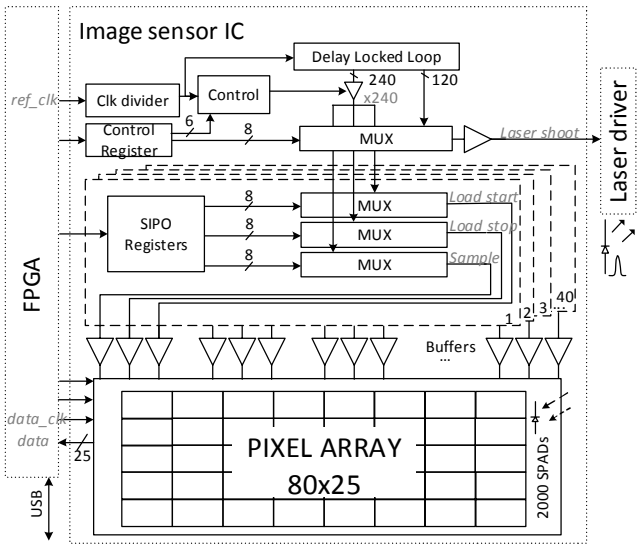

Fig. 5. Block-level representation of the imaging system. Note separate timing controls for 40 SPAD sub-arrays.

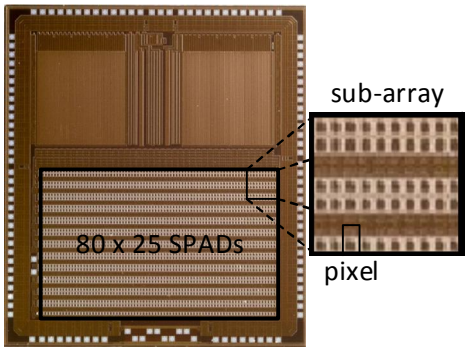

Fig. 6. Picture of the chip.

V. MEASUREMENT RESULTS

A 3D range image of two spheres is shown in Fig. 7. The diameters of the targets with non-cooperative surfaces are 30 cm and 11 cm and they were placed at the distances of 80 cm and 60 cm from the transceiver. The positions of the time gates at the beginning of the scan are shown in Fig. 7 a) and a partial scan range of 30 cm with ~1.5 cm (~100 ps) LSB z-resolution was selected. The time gate widths were 800 ps. The shown result was achieved by using 1000 laser pulses for each of the time gate positions (i.e. 20 000 laser pulses for the 30 cm partial scan). The laser pulsing rate was 100 kHz resulting in a 3D frame rate of 5 Hz. The laser pulse had a wavelength of 860 nm, an energy of ~1 nJ and FWHM of 110 ps. An optical bandpass filter was placed in front of the detector lens to suppress the ambient light. The measured ambient lighting at the object FOV was 200 – 600 lux. The current consumption of the receiver from a 3.3 V power supply is 20 mA of which 5 mA is consumed by the delay-locked loops and the time gating circuitry.

VI. CONCLUSIONS

A time gating topology for solid state 3D scanning with a CMOS SPAD imager is presented. The topology is based on two on-chip delay-locked loops which have altogether 240 outputs from which the time gating signals can be selected. The 2D SPAD array has been divided into 40 sub-arrays whose time gating can be programmed individually from the delay line outputs with 8 bits. The measurement results show functionality of the topology and the detector's insensitivity to normal office lighting with 800 ps time gate widths. The fabricated imager has 80 × 25 pixels in a sensor area of 4 mm × 2.5 mm with a 32 % fill factor which is remarkable for a large (>1000) SPAD array without the use of micro lenses. A 3D range image rate of ~5 fr/sec with ~cm precision is demonstrated to passive targets within a range of ~1 m and 36 x 57 degrees FOV. The result compares quite favorably with the state of the art [8] taking into account the large FOV and much lower illumination power (average 0.1 mW) and receiver aperture (~3.5 mm).

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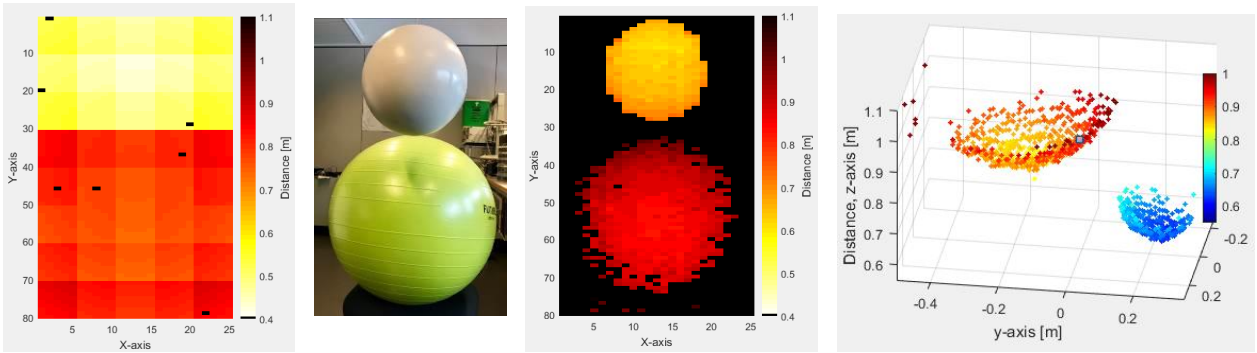

Fig. 7. a) Position of the time gates and eliminated noisy pixels at the start of the scan, b) picture of the targets, c) distance result of the pixels and d) 3D image of the targets.