Performance Improvement of Multi-Stacked CMOS mm-Wave Power Amplifiers Based on Negative Capacitance Phase Compensation

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***Abstract*— This paper proposes a method for performance improvement of multi-stacked CMOS millimeter-wave power amplifiers based on negative capacitance phase detuning, which can be generalized to other phase detuning techniques. It not only yields better inter-stage matching between stacks, but also offers the advantage of relaxed inter-stage phase rotation due to transistor parasitics. A ×1.6 output power/gain and 7% efficiency improvement is observed as a result of the proposed technique. This is achieved because phase misalignment between stacks is minimized. The method is evaluated using simulations based on 28GHz PA in 45nm CMOS technology.**

Keywords—CMOS; millimeter wave integrated circuits; power amplifier; stacked transistor;

I. INTRODUCTION

The need for fully integrated efficient millimeter-wave PAs has led motivation for CMOS based PA design. However, low breakdown level of scaled CMOS transistors yields limited obtainable amount of power from a single transistor. To overcome the issue, stacking transistors was proposed, [1]–[4]. Due to the presence of transistor parasitics, though, stacking topology requires additional networks for inter-stage matching and phase alignment of each and every amplifier stage in order for the signals to be efficiently superimposed up to the output node [5]–[8]. In this respect, the current paper presents a novel method based on negative capacitance parasitic effect cancellation which yields reduced phase rotation along the stacks and hence inter-stage phase misalignment, which improves the overall PA performance.

II. STACKED CMOS DEFINITION AND RECENT APPROACHES FOR INTERMEDIATE INTER–STAGE MATCHING

A typical schematic of a stacked CMOS PA topology is shown in fig. 1. The capacitances C_2 – C_N are designed so that the desired optimal load-line defined by R_{opt} is guaranteed while a part of signal swing is allowed at the gate nodes. This way, the signal swing across each junction, i.e. V_{DS}, V_{GS}, and V_{DG}, is limited to be within the breakdown constraints. By superposition theorem $V_{out} = NV_{D1}$.

The presence of transistor parasitics pose mismatching between stages and phase shift at the output of each stack, which yields the overall amplitude reduction, hence output power and efficiency [9].

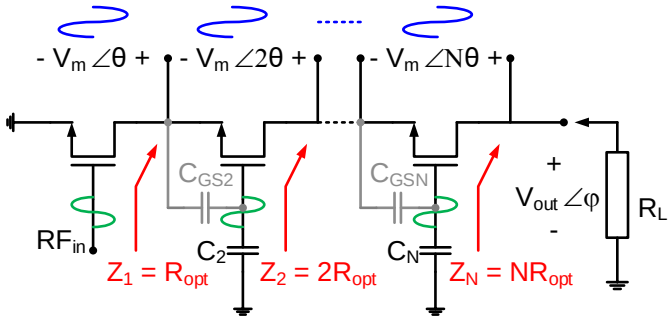

Fig. 1. Typical stacked CMOS transistor PA configuration.

Thus, some phase detuning mechanism is required to improve the performance of the PA device. Three main tuning techniques are shown in fig. 2. Use of a series inductance between two-stacked-transistors (Fig. 2(a)) to cancel the imaginary part of the input impedance was mentioned in [6]. In order to resonate out the parasitics [7] proposed a shunt inductance tuning technique (Fig. 2(b)). [8] Proposed a shunt capacitor tuning technique, which was fed back from drain to source (Fig. 2(c)).

III. PROPOSED INTER-STAGE MATCHING METHODOLOGY

The above-mentioned methods still lack the required design accuracy as part of parasitics were neglected. Using the high frequency transistor model (fig. 3(a)), and neglecting the effect of r_o, the input impedance of the n+1st stack, is expressed as

$$Z_{in_n} = \frac{1}{(g_m + sC_{gs})} \times \frac{\begin{pmatrix} C_{gs} + C_{gd}(1 + g_m(n+1)R_{opt}) + C_{n+1} \\ + sC_{gd}(C_{n+1} + C_{gs})(n+1)R_{opt} \end{pmatrix}}{(C_{gd} + C_{n+1} + s(n+1)R_{opt}C_{n+1}C_{gd})} \quad (1)$$

which is used in dimensioning gate capacitances C_n [4], [5], [8]. The frequency dependent nature of Z_{in} forces gate capacitances, C_n, to be variable with frequency, which is not feasible. This is the very first origin of discrepancy.

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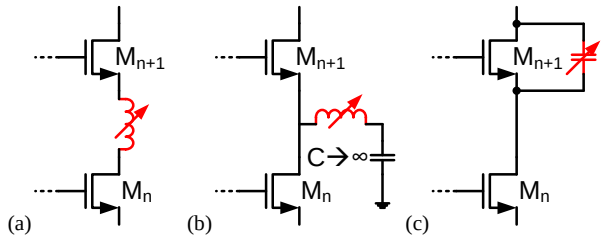

Fig. 2. Inter-stage matching networks, a) series inductive tuning, b) shunt inductive tuning, c) shunt capacitive feedback tuning.

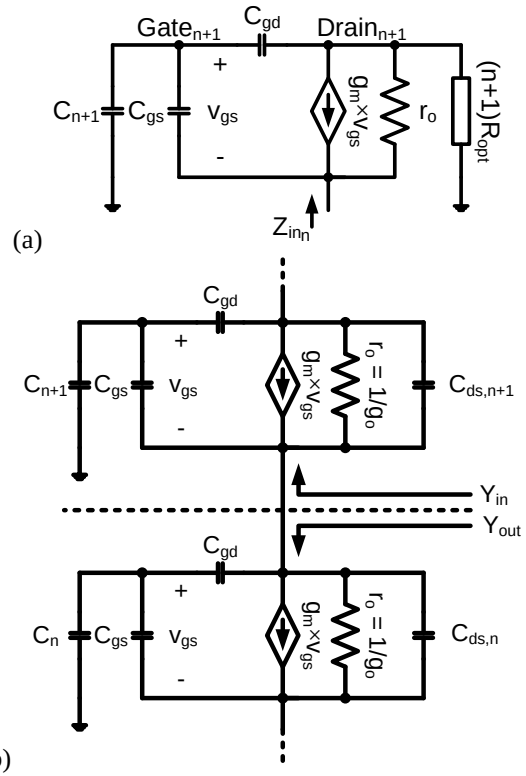

Fig. 3. high frequency CMOS transistor model a) used for dimensioning Cn, and b) used for inter-stage admitance calculation.

Moreover, the susceptances looking upwards and downwards are not conjugately matched in general (fig. 3(b)). Calculating the mentioned susceptances, we have

$$\mathrm{Im}(Y_{in}) = \frac{\omega}{n}\left(\frac{C_{gs}}{g_m R_{opt}} - C_{ds_{n+1}}\right) \tag{2}$$

$$\mathrm{Im}(Y_{out}) = \frac{\omega}{n}\left(\frac{C_{gd}}{g_m R_{opt}} + C_{ds_n} + C_{gd}\right). \tag{3}$$

It is immediately seen from (2) and (3) that another design inaccuracy originates from the discrepancy between the susceptances seen towards different directions, which must be compensated for. The above issues were neglected in [4]–[8], when dimensioning devices, whereas the rest of this section is devoted to address it.

A closer look at (2) and fig. 3(b) reveals that $C_{ds,n+1}$ is gyrated to be negative. If its value is chosen to be equal to $C_{gs}/g_m R_{opt}$, the frequency dependence requirement of C_n is removed, however (3) poses more phase rotation. Equating (2) to negative of (3) fully removes the frequency variable requirement as well as non-conjugate-equal imaginary parts. Thus

$$\frac{\omega}{n}\left(\frac{C_{gs}}{g_m R_{opt}} - C_{ds_{n+1}}\right) = -\frac{\omega}{n}\left(\frac{C_{gd}}{g_m R_{opt}} + C_{ds_n} + C_{gd}\right). \tag{4}$$

Solving (4) for $C_{ds,n+1}$ with $C_{ds,1} = 0$, results in

$$C_{ds_{n+1}} = n \times \left(\frac{C_{gs} + C_{gd}}{g_m R_{opt}} + C_{gd}\right). \tag{5}$$

The dimensioning rule of (5) guarantees proper phase cancelation along the stack. Although the calculations were performed for proposed negative capacitance compensation method, without loss of generality, the approach can be applied to other detuning techniques introduced in [4], [5], and [8]. More importantly, $C_{ds,n+1}$ can be dimensioned to compensate for more parasitics in order for more phase compensation purposes.

With the removal of the frequency dependency of the input impedance, (1) can be made equal to nR_{opt} and solved for C_n. Thus,

$$C_{n+1} = \frac{C_{gs} + C_{gd}(1 + g_m R_{opt})}{g_m n R_{opt} - 1} \tag{6}$$

which is consistent with [5]. Using dimensioning rules (5) and (6) concurrently preserves the resistive property of load-lines to a higher extent. This gives rise to overall PA performance improvement, i.e. output power, power gain and efficiency [9].

Due to the fact that more parasitics are taken into account when designing $C_{ds,n}$, the proposed method accounts for 10% to 20% more accuracy in the design and simulations compared to the approaches explained in [1]–[8].

IV. Simulation Results

To verify the proposed design methodology, a four-stack CMOS PA was designed and simulated based on 45nm CMOS technology (Fig. 4). The operating frequency was chosen to be 28GHz which is a candidate band for 5th generation wireless communications systems.

The PA was dimensioned to provide 100mW to a 50Ω load, i.e. R_{opt} = 12.5Ω. Biasing network of $R_1 - R_5$ were chosen to be much higher than the $C_2 - C_4$ impedances at the desired frequency band. The device finger length was chosen to be 560nm with total 40 fingers. The transistor parameters are: I_D = 63mA, g_m = 350mS, C_{gs} = 200fF, C_{gd} = 45fF, r_o = 65Ω, $R_1 - R_4$ = 17.46kΩ, R_5 = 20kΩ, R_L = 50Ω, R_{opt} = 12.5Ω, V_{DD} = 3.15V.

Simulations quantifies an approximately 14% deviation between simulation and analytical impedance. The nonlinearity of the parasitics, i.e. AM-PM distortion, is the reason for such phase variation.

The phase rotation per stack and the total phase shift at the output of the nth stack are illustrated in fig. 5. It can be implied that the proposed method has introduced a 20% improvement in phase alignment between the stacks.

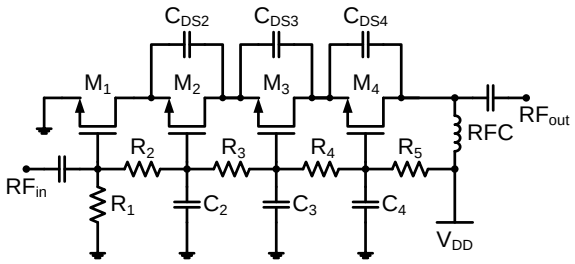

Fig. 4. Schematic of the designed 4-stacked mm-wave PA circuit.

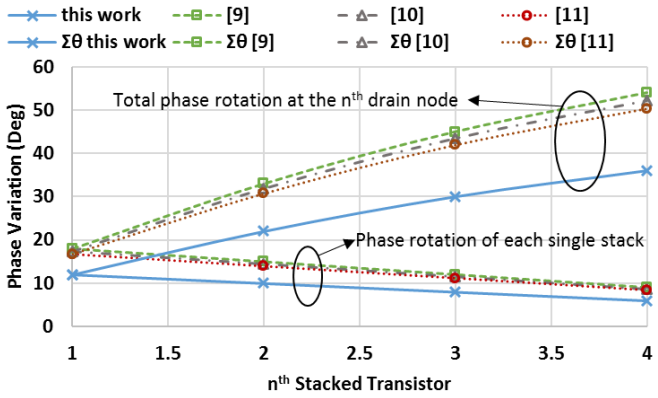

Fig. 5. Total phase rotation at the output of the nth stage as well as phase rotation posed by every single stage.

The load-lines of fig. 6 resemble resistive behavior to a very good extent. A gradual increase in voltage swing is also observed along the stacked transistors (Fig. 6), while the current swing remains constant through them. This is consistent with the impedance growth concept explained in the schematic of fig. 1.

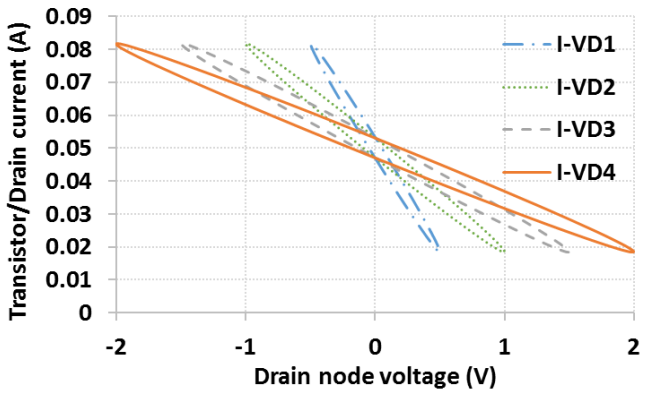

Fig. 6. Load – line simulation result of each drain node.

Fig. 7 illustrates the large signal behavior of the designed PA before and after utilizing the proposed method, which proves the validity and value of the proposed method. From Fig. 7, it can be seen that output power, power gain and drain efficiency (DE) are improved after removal of the effect of the parasitics based on negative capacitance phase compensation. A 2dB increase in power gain as well as output power and 7% increase in drain efficiency was achieved which verifies the significance of the proposed method.

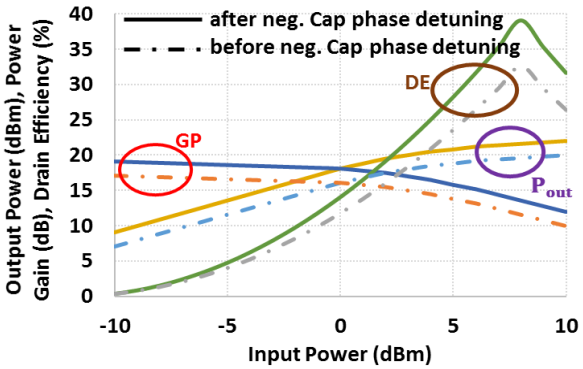

Fig. 7. Performance improvement offered by the peoposed method.

V. Conclusion

A theoretical design method for stacked-CMOS PA based on negative capacitance phase detuning was proposed in this paper. It is also general enough to include more parasitics into account in case needed. By virtue of the method, the reactive part of the impedance seen at each drain node as well as phase rotation per stack were minimized. Thus, a superb phase alignment between each of the stages in the stack was achieved, which is desirable for appropriate stacked PA operation. Based on the proposed method, a 28GHz PA was designed and simulated. The simulation results proved the excellence of the technique in the design of such PAs.

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