Design of Stacked-MOS Transistor mm-Wave Class C Amplifiers for Doherty Power Amplifiers

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***Abstract* — This paper discusses the design requirements of class C auxiliary (aux) amplifiers deployed in Doherty power amplifiers (DPA). Taking conduction angle and back-off (BO) level into account a global design chart is presented which can be utilized to properly dimension the aux amplifier. Based on the proposed method a class C power amplifier is designed and exploited in a DPA circuit at 28GHz which is evaluated using simulations based on 45nm CMOS technology. Simulations reveal 27dBm saturated output power, 60% maximum drain efficiency (DE), 45% DE at 6dB BO, and 2 times efficiency enhancement at 6dB BO which is a new record in this trend.**

***Keywords* — CMOS integrated circuits, millimeter wave integrated circuits, Doherty power amplifier, class C amplifier.**

I. Introduction

The higher bandwidth and data rate offered by millimeter wave (mm-wave) spectrum has attracted the attention of industries and academic research units in order to work out the viability of implementing the next generation of high data rate systems such as 5G, IoT, etc. [1]–[3].

The none-constant envelope property of the high order modulation schemes deployed in the foregone systems puts strict circuit design requirements including particularly power amplifiers (PA) as the key building block of transmitters (Tx). As the ultimate performance of a Tx is dominated by its PA special care needs to be taken when designing a PA, i.e. existence of high peak-to-average-power ratio (PAPR) entails linearity while keeping efficiency at the back-off (BO) conditions. In fact, this translates to both excess power consumption and in turn thermal management in base stations (BS) which prevails system operation cost. In addition, PA efficiency renders in battery lifetime expectancy issue in the handheld devices. Whereas standalone linear PAs, i.e. class A/AB/B, pose poor efficiency at BO conditions, Doherty PA (DPA) topology offers reasonable performance at the mentioned conditions.

This has led to a research focus on the development of mm-wave DPAs. Due to high power density and moderate thermal behavior, compound semiconductor MMICs have been the preferred choice for such amplifiers for several years. But when it comes to cost efficient fabrication as well as integration level, CMOS technology is the prime choice [4] – [6].

Nonetheless, low breakdown level of scaled CMOS transistors yields limited obtainable amount of power from a single transistor. In order to overcome the mentioned problem, stacking transistors in series connection on top of each other was proposed [1]–[3], [7]–[9].

Most of the proposed stacked-transistor structures are based on a standalone PA to operate in a fixed class A/AB/B condition, which were utilized as the main amplifier, but, to the authors' best knowledge, not as the auxiliary (aux) amplifier in a DPA structure. In addition, not many literatures have been dedicated to explore the impact of the aux amplifier characteristics on the ultimate performance of the DPA structure. This paper is devoted to bridge this gap and using stacked-CMOS topology introduce an aux amplifier design/dimensioning rule for DPA structures. It should be noted that the effect of parasitic elements on the performance of each single amplifier is discussed in [7] based on which one can predict the impact of parasitics on the overall performance of DPA.

In this regard, the effect of aux amplifier on the overall DPA structure is discussed in section II. Section III concerns the design requirements of the aux amplifier. Afterwards, using the proposed methodology a class C amplifier is designed and evaluated in a DPA framework in section IV.

II. The Effect of Aux Amplifier on the Overall DPA Structure

In order to be able to explore the impact of aux amplifier on the overall efficiency of the DPA device a 4-stack CMOS class AB amplifier was designed with the performance characteristics shown in fig. 1.

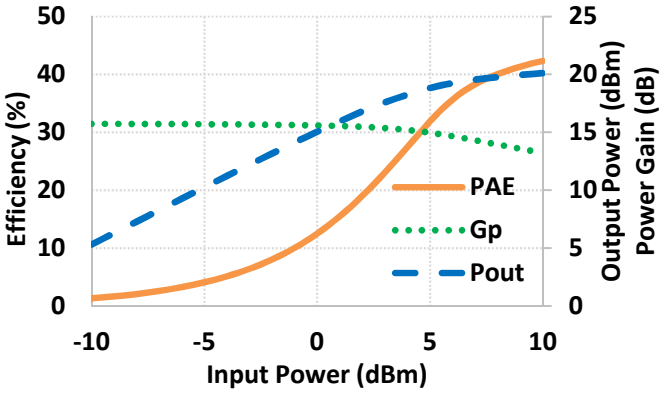

Fig. 1. Performance characteristics of the class AB amplifier exploited as the main amplifier in DPA.

Also the aux amplifier was replaced with an ideal piecewise linear voltage controlled current source (vccs) shown in fig. 2, wherein K, $V_{turn\text{-}on}$, and V_{sat} represent the linear transconductance gain, the level at which the vccs starts to conduct, i.e. turn-on point, and the level at which the output of vccs saturates, respectively.

The effect of aux amplifier characteristics on the load modulation and the overall DPA power added efficiency (PAE) are depicted in fig. 3 and fig. 4.

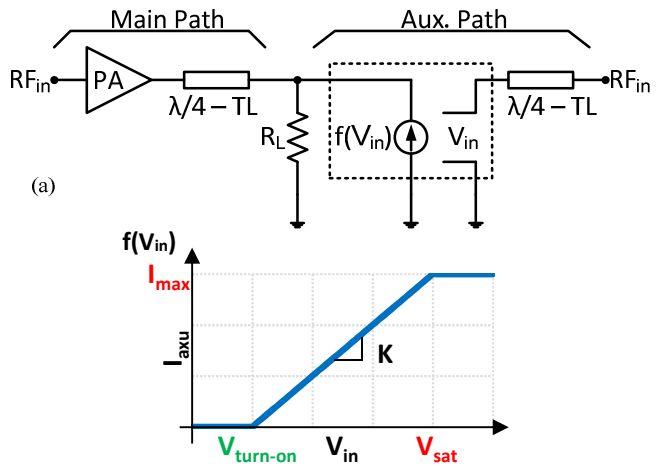

Fig. 2. a) DPA with ideal piecewise linear vccs, b) I-V characteristic of vccs.

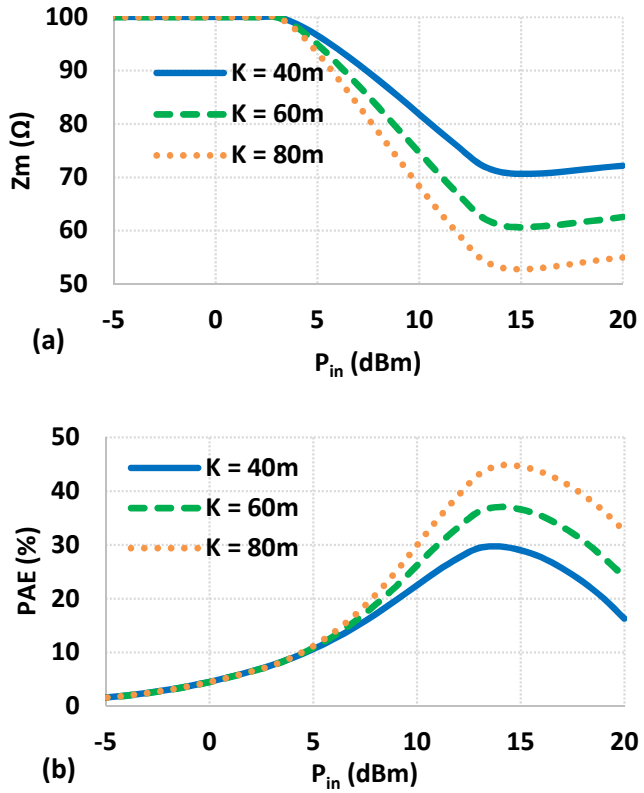

Fig. 3. a) Load modulation seen by the main amplifier and b) the overall DPA PAE as a function of the aux amplifier K.

Fig. 3 illustrates the effective load modulation as a function of the aux amplifier transconductance K. Based on the DPA operating principle, in case the aux amplifier is incapable of suppling enough current into the load, the pulled load seen by the main amplifier is not optimum and therefore the required signal swing is not reached. As a result the efficiency drops even though a second amplifier has been utilized.

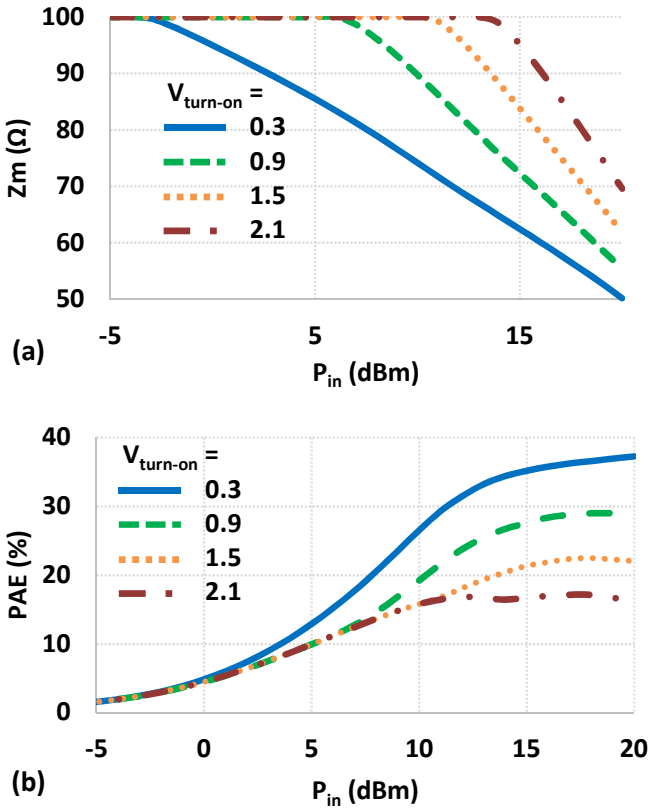

Fig. 4. a) Load modulation seen by the main amplifier and b) the overall DPA PAE versus different biasing conditions.

The impact of turn-on point, $V_{turn\text{-}on}$, on the load modulation and PAE is shown in fig. 4. It can be directly deduced that even a properly dimensioned aux amplifier may not be able to supply enough current essential for appropriate load modulation, if it is not biased correctly, which directly impacts the final performance. In other words, the deeper the aux amplifier is in class C, the less it is capable of injecting current into the load. This is inevitable as the conduction angle determines the amplitude of the first harmonic of the aux amplifier's current.

Accordingly, although, at lower power levels the main amplifier dominantly defines the overall DPA performance, the aux amplifier characteristic can influentially dominate the performance of the overall DPA at higher power levels.

III. Design Methodology of the Aux Amplifier

Due to velocity saturation and mobility degradation instead of a square law property, nano-scaled MOS transistors tend to show a linear dependence on drive signal. Thus,

$$I \propto \frac{W}{L}(V_{GS} - V_{th}) \qquad (1)$$

is assumed in the following.

As mentioned earlier, lack of current projected into the load by the aux amplifier gives rise to insufficient load modulation [10] at the desired power levels required to be seen by the main amplifier. This yields lack of power delivered to the load and in turn pulls down the efficiency at higher power levels. According to (1) the current amplitude can be adapted by both device dimensions, i.e. W/L aspect ratio, as well as biasing conditions V_{GS} compliant with $V_{turn\text{-}on}$. While the aspect ratio directly impacts the current amplitude, the biasing condition defines the conduction angle.

As the output current of the class C amplifier is a clipped sinusoidal signal (fig. 5), the existence of harmonics are unavoidable. Hence, Fourier analysis is required to calculate the device dimensions based on conduction angle. Thus

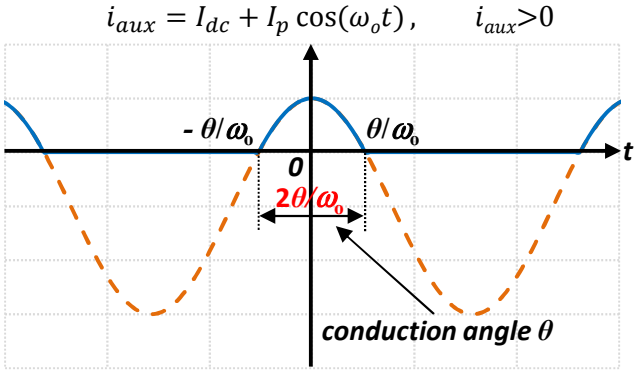

Fig. 5. Aux amplifier output current waveform

$$I_{aux} \cong I_{DC} + \sum_{n=1}^{\infty} I_n \cos(n\omega_o t) \quad (2)$$

where I_n is defined by Fourier integral as follows

$$I_n = \frac{\omega_o}{\pi} \int_{-\theta/\omega_o}^{\theta/\omega_o} (I_{dc+} I_p \cos(\omega_o t)) \cos(n\omega_o t)\, dt \quad (3)$$

and θ is the angle at which the aux amplifier turns on which is expressed as

$$\theta = \cos^{-1}\left(-\frac{I_{dc}}{I_p}\right) = \cos^{-1}(V_{turn-on}/V_{max}). \quad (4)$$

As the fundamental component is of interest, all higher harmonics and the dc component are truncated using resonator circuits. Solving (3) for the first harmonic, i.e. $n = 1$, we have

$$I_1 = \frac{I_p}{2\pi}(2\theta + \sin(2\theta)). \quad (5)$$

(5) Explains how the fundamental component of the class C aux amplifier departs from its class A main amplifier as a function of conduction angle when the dimensions kept constant (see fig. 6). In order for I_1 to catch up with the fundamental component of the main amplifier, i.e. I_p, the aux amplifier needs to be re-dimensioned as follows

$$\left(\frac{W}{L}\right)_{Aux} = \frac{2\pi}{2\theta+\sin(2\theta)} \times \left(\frac{W}{L}\right)_{main}. \quad (6)$$

In order to extract (6), the main amplifier was supposed to be in class A operating conditions which is not the case in general. Conversely, class AB/B are preferred in DPA topologies which means the conduction angle of the main amplifier may not necessarily be 360°. Following the same procedure explained in (3) – (7) for different conduction angles along with different $V_{turn\text{-}on}$. In other words, we can vary the conduction angles of both main and aux amplifiers, and just choose their appropriate aspect ratios, i.e. W/L, so that their fundamental sinusoidal amplitudes are equal. If the calculations are normalized to I_p of class A amplifier, the main/aux amplifier ratio of the normalized ratios will give the appropriate W/L for proper operation. This is globally done in design chart of fig. 6 and will be exemplified in the following.

The design chart of fig. 6 proves as a useful graphical tool for aux device dimensioning in the sense that knowing the conduction angle of the main amplifier, its normalized maximum fundamental component amplitude of the output current can be predicted. From there the effect of $V_{turn\text{-}on}$ and hence BO condition on the same device utilized in class C is estimated. Once this is at hand, the required device dimensioning can be immediately approximated using the chart.

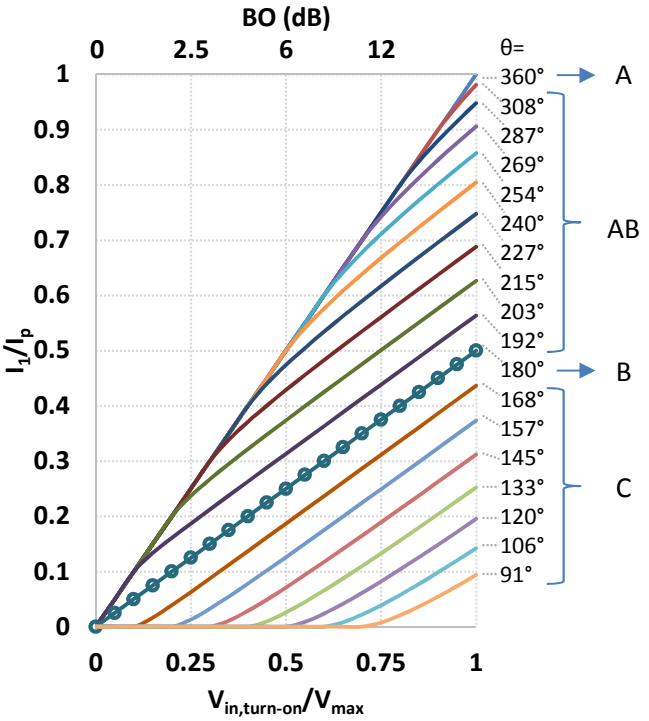

Fig. 6. Global design chart used for aux amplifier dimensioning based on the main/aux amplifiers conduction angles, break point level and/or BO conditions.

An example will clarify the above statement. Suppose the main amplifier is biased such that it is in class A operating condition, i.e. θ = 360°. In order for the load to be successfully modulated at 6dB BO region, i.e. θ = 120°, a ratio of 1 to 0.2 is seen in the chart. Thus the aux amplifier dimension should be 5 times that of the main amplifier. Or in another example, if a

12dB BO is desired with the same main amplifier, a ratio of 1 to 0.1 is seen in the chart which means that the aux amplifier aspect ratio should be 10 times that of the main amplifier.

Also part of the dimensioning rule proposed in chart of fig. 6 can be relaxed if the aux amplifier input can be driven asymmetric compared to the main amplifier. This can be done using asymmetric power dividers. For example if the input drive of the aux amplifier is 2 times the main amplifier input drive, the aux amplifier dimensions can be halved.

To summarize, the design procedure starts with the definition of the current amplitude by the required power to be delivered to the load. This is the maximum current/power level that both main and aux amplifiers must reach which should be normalized to the maximum current of a 360° conducting main amplifier. Following that, the break point where the aux amplifier turns on must be defined, i.e. the BO level. Based on the BO level, using global chart of fig. 6, the proper biasing along with conduction angle of the transistors can be estimated. Based on the conduction angle of the transistors the aux amplifier device dimensions are calculated using the same global chart of fig. 6. The above design procedure is depicted in the design flow chart of fig. 7.

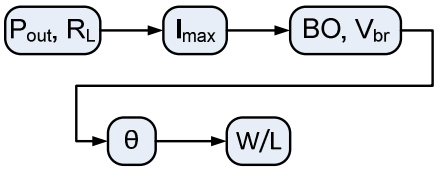

Fig. 7. Design flow of aux amplifier

IV. Design Example and Simulation Results

Using the proposed method, a 4-stack aux amplifier was design using CMOS 45nm technology at 28GHz operating frequency. Both the main and the auxiliary amplifies share the same circuit schematic which is shown in fig. 8. The capacitances C_2 – C_4 were dimensioned using the method presented in [6]. The main amplifier was biased in class AB with a simulated conduction angle of nearly 260°. The device finger length was chosen to be 560nm with total 40 fingers, the performance characteristics of which is depicted in fig. 1. The fundamental current component of the main amplifier was simulated to be 90mA, i.e. $I_{1_{main}} = 90mA$.

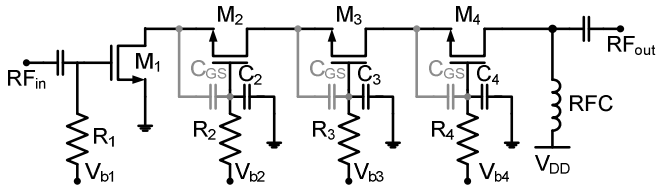

Fig. 8. Simplified circuit schematic of the main and aux amplifiers

The rest of this part is devoted to design a proper aux amplifier so that the overall DPA delivers 27dBm power to a load of 50Ω while keeping efficiency high at the 6dB BO region. The power requirement reveals that each amplifier is required to supply current amount of 90mA. As can be seen from the chart of fig. 6, the 6dB BO condition points to 0.2 of I_1/I_p and 260° of conduction angle points to 0.8; thus, in order for the aux amplifier to be able to supply the required current into the load, the dimensions need to be quadrupled, i.e. ≈ 0.8/0.2.

As previously stated, it is also possible to relax the dimensioning rule. If the drive to the aux amplifier is 2 times that of the main amplifier the dimensions of the aux amplifier can be halved. The main and aux amplifiers currents are shown in fig. 9. It can be immediately seen that the design requirement is met and the required load pull/modulation is guaranteed.

Shown fig. 10 is the output power of the DPA circuit based on the designed class C amplifier. It can be observed that the required output power of 27dBm is achieved and it is two times, i.e. 3dB higher than, the single standalone class AB PA.

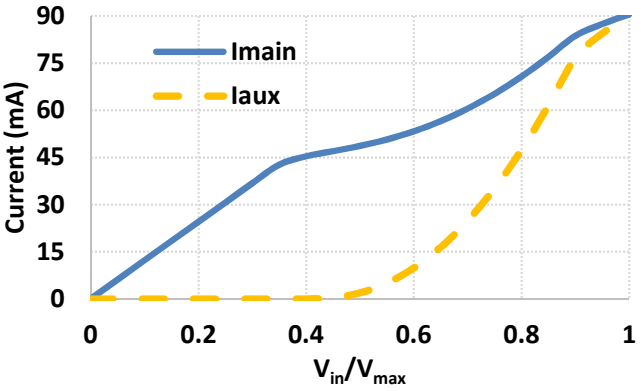

Fig. 9. Main and aux amplifiers'

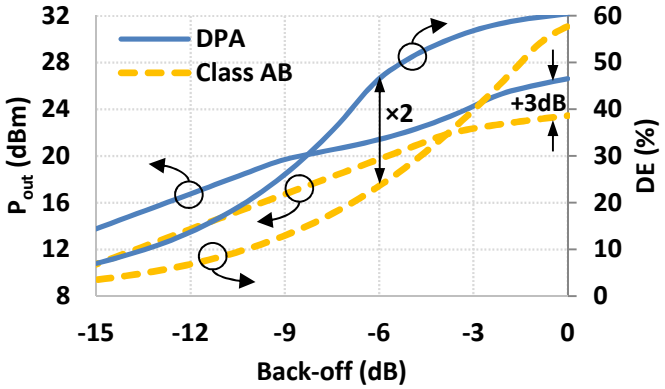

Fig. 10. The output power and drain efficiency (DE) of the overall DPA using the designed aux amplifier based on the proposed method.

More importantly, fig. 10 illustrates the drain efficiency of the DPA compared to its class AB counterpart. An efficiency improvement of ×2 can be seen at 6dB BO which is desirable. To the best of the authors' knowledge this is the highest reported efficiency enhancement factor compared to the latest state-of-the-art published CMOS DPA structures [4] – [6].

V. Conclusion

A global design chart was invented in this paper for the first time, which provides several different information on trade-offs between BO, conduction angle, biasing, and current projection in class A, AB, B, and C PAs (whether exploited as standalone PAs or as main/aux amplifiers in DPAs).

In other words, the proposed chart visualizes the main and aux amplifiers normalized output current capability at a diverse set of biasing and BO conditions. The ratio of the normalized output currents indicates a scale factor which can be utilized to re-dimension the aux amplifier with respect to its main counterpart. This way a proper load modulation presented to the main amplifier is guaranteed. Several cases were exemplified to support the above statements.

By means of the proposed chart, a class C amplifier was designed and deployed in a DPA configuration and evaluated. The results of the simulations showed a doubling improvement in efficiency at 6dB BO which proves the value of the proposed methodology.

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