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# Continuously controlled and discrete-level charge pumping techniques implemented in SC integrators

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**Abstract**
This paper presents two methods to reduce power consumption of switched capacitor (SC) integrators in sigma-delta analog to digital converters. The proposed two methods are based on the passive charge re-distribution technique, injecting charge into the output of the first integrator. The injected charge can be attained by a continuous function of the input voltage and feedback, or by quantizing the injected charge into three levels. In both cases, the main purpose is to minimize the initial transient voltage at the input of the first operational transconductance amplifiers (OTA), in order to bypass the slewing region of the OTA and enter into the linear settling region. Then a minor charge is left, and needs to be moved by the OTA. Using these two charge pumping techniques separately, a 10-bit performance of a conventional second-order delayed cascaded 1-bit sigma-delta modulator which consists of two SC integrators can be obtained by only consuming 60% power dissipation of the traditional structure without proposed techniques.

**Keywords** Switched capacitor · Slew rate · Initial input voltage · Current pumping · Power saving

## 1 Introduction

Switched-capacitor (SC) circuit use Operational Transconductance Amplifier (OTA) to transfer charge on capacitors around OTA. Charge is moved dominantly by the OTA. Right after the switching, the total charge is passively re-distributed, results in large initial transient voltage spikes (Vi0) at the input of the OTA. If the initial voltage step Vi0 exceeds the linear input range of the OTA, it drives the OTA into the slewing. The time spent in slewing is taken away from the linear settling time, causes high non-linear settling error.

A major design bottleneck is that the compromise between faster settling speed and power consumption reduction. Numerous ways to either enhance the class AB operation of the OTA or to make its bias current signal time-dependent can be found in the literature [1–6]. Dominantly they affect the internal design and dimensioning of the OTA itself. This paper proposes an open-loop charge injection technique that is completely outside the OTA, hence it does not affect its dimensioning, noise or offset property, and it does not cause any new internal time constants. Yet it minimizes the initial transient voltage input to the OTA, therefore avoids the slewing period, which makes it possible to considerably reduce the bias current. In [7], injected charge is implemented by a passive capacitive pulling technique which was introduced a pre-charged load capacitor into a SC residue OTA. But this technique is not applicable to integrator circuit topologies that preferably have disconnected loads during the evaluation phase. Therefore, a new idea of implementing a pulsed current injection into the output node of the OTA during the integration phase is presented here.

Section 2 of this paper describes the charge redistribution technique used in SC integrator and gives an overview of various methods that injects a pre-calculated charge (Qpre) into the integrator. Section 3 presents the circuit level implementation of a dynamically and continuously controlled current pumping (CP) circuit. Section 4 shows the simulated results of applying the continuously controlled current pumping technique to a second-order sigma-

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delta modulator (SDM), and analyzes the effects on power consumption. Similarly, Sects. 5 and 6 present the circuit implementation of the three-level current pumping circuit, and its effect on power consumption in the second-order SDM.

## 2 Charge redistribution power saving technique

The common second-order delayed cascaded 1-bit SDM is shown in Fig. 1. During the integration phase, the OTA transfers the charge via S2 and S4, the output of each stage approaches the final value determined by the integrator transfer function. The charge sharing causes large and signal-dependent initial voltage steps at the input of the OTAs. At the very beginning of the integration phase, a pre-calculated charge (Qpre) is added to the output of the first OTA. It is assumed that the OTA itself has no effect yet, but the total charge is passively and almost immediately redistributed. Injected Qpre helps to move the charge, so that Vi0 of the OTA is forced to close to zero instantaneously after Qpre injection. Therefore, the OTA bypasses the non-linear slew rate limited region and has only a minor linear correction to do. The current delivered by the main OTA can be largely decreased compared to the conventional structure. Figure 2 shows the capacitors connection of the first stage at the end of the sampling phase and at the beginning of integration phase using alternative charge injection techniques.

To understand the operation of the proposed implementations, we repeat some part that was explained given in [7] and calculate the expression of the required charge injection (Qpre). It is assumed that the charge sharing occurs quickly enough that the OTA has no significant effect on moving charge. Therefore we assume that the charges in node A or B in Fig. 2 at the end of the sampling and at the beginning of the integration period are the same. By equivalating the charges in node A and B at the end of the sampling and at the beginning of the integration period, the initial voltages Vi0 and Vo0 can be determined. This gives the sum of charge equations (1), where Vin is the input voltage sampled in C1, Vref is the feedback voltage where C2 is connected to during the integration phase, Vop is the previous output voltage of the first stage and Qpre is the required charge injected into the output node.

$$\begin{aligned} A &: C1 \times (Vi0 - 0) + C2 \times (Vi0 - Vref) + C3 \times (Vi0 - Vo0) \\ &= -Vin \times C1 + 0 \times C2 - C3 \times Vop \\ B &: C3 \times (Vo0 - Vi0) = C3 \times Vop + Qpre \end{aligned} \tag{1}$$

Now we can solve Qpre by setting Vi0 is zeroed. By injecting the Qpre, the majority of the charge is essentially moved before the OTA starts its work. Qpre expression is simple, as seen:

$$Qpre = Vin \times C1 - Vref \times C2 \tag{2}$$

Four methods of implementing the required charge Qpre are shown numbered in the right side of Fig. 2. The method of connecting an additional pre-charged capacitor Cext (method 3) at the output of the SC integrator results in impractically high pre-charge voltage values. Hence, the idea of injecting current pulses to the output is practical. The total charge Qpre can be controlled either by a current magnitude (Ipump of Fig. 2: method 1) or by a pulse duration $\Delta t$ which is shown in Fig. 2: method 2). From the settling point of view, the former one is easier, as it has a fixed duration of $\Delta t\_fix$ (here 1.5 ns). When aiming for complete cancellation of Vi0, the magnitude Ipump of the fixed-duration current pulse needs to be dynamically controlled. Assuming a trapezoidal pulse with a rise and fall time and duration of tr, tf, and tw, respectively, $Qpre = Ipump \times (tr + tw + 2tw)/2$. From that, the pump current can be solved according to the following equation:

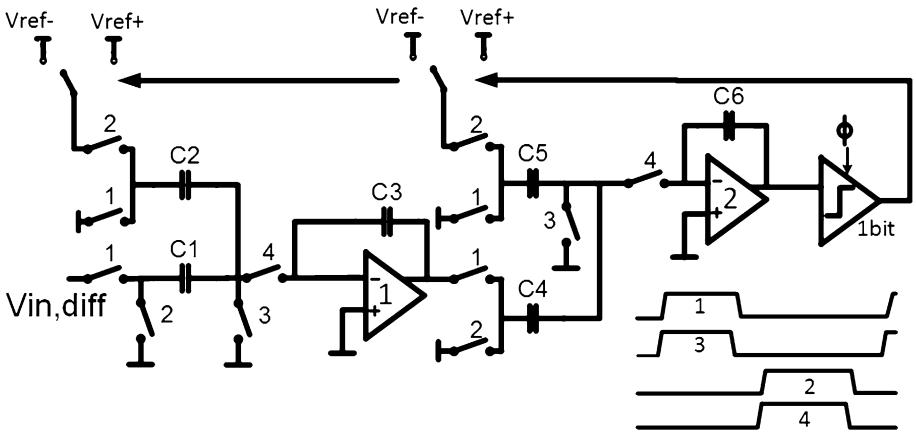



**Fig. 1** Schematic and phase arrangement of the conventional SDM structure

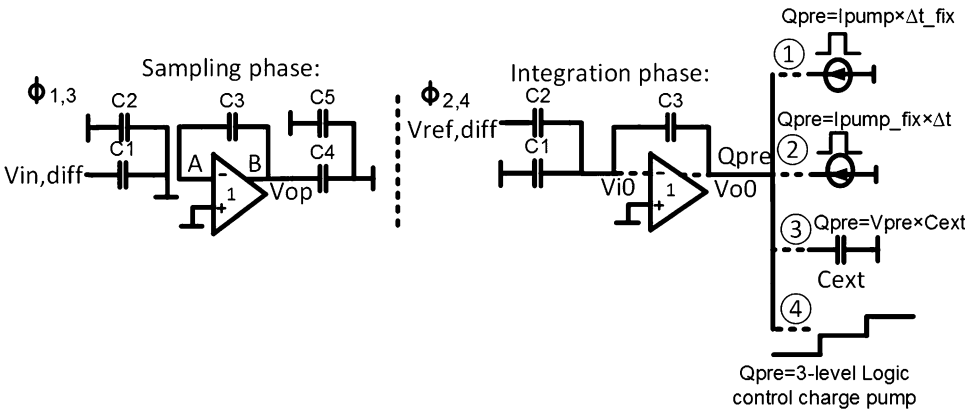



**Fig. 2** Setups for solving charge equations in nodes A and B (1–4 are alternative charge injection techniques)

$$Ipump = (Vin \times C1 - Vref \times C2)/(0.5tr + 0.5tf + tw) = K1 \times Vin - K2 \times Vref \quad (3)$$

A technically simpler approach is to quantize the injection current to a few values, as illustrated in Fig. 2: the 4th method. The dark blue curve and the green curves in Fig. 3 represent the required amount of charge needed according to (2) when the reference voltage is 1.2 V or − 1.2 V. Using just the Vref polarity information reduces the Vi0 to half of original value, allowing for sufficient quantization of Vin with three levels. Vin quantization can be done by simple dynamic comparators. Using this 3-level injection, a residual charge Qremain (shown in Fig. 3) is left, and it is small enough to bypass the slewing behavior.

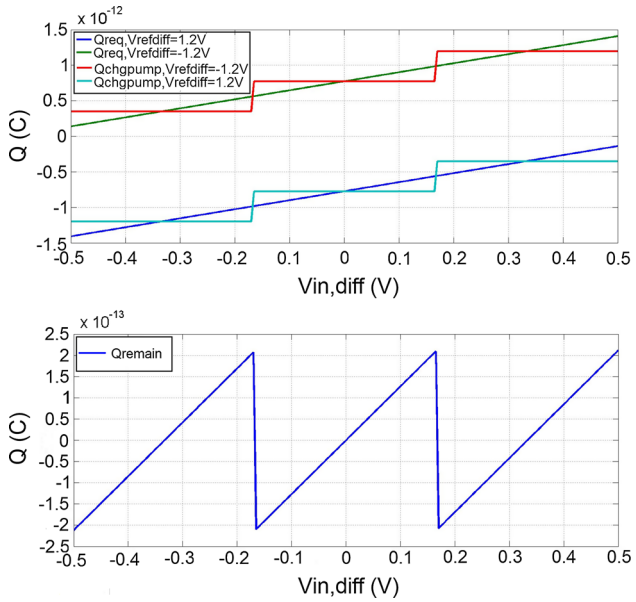



**Fig. 3** The required charge and the charge pumping levels

## 3 Implementation of the continuously controlled current pulse source

The continuously controlled current pumping circuit uses instantaneous values of Vin and Vref to generate Qpre in order to minimize Vi0. It consists of three main parts as shown in Fig. 4. The first part is a transconductor amplifier stage which converts the input voltage to a current $\Delta i = k1 \times Vin$. The second part subtracts or adds $|\Delta i|$ from a fixed current with a magnitude of $|k2 \times Vref|$, and generates the needed pulse magnitude ipump. The third part generates the actual pumping current Ipump shown in Eq. (3) by amplifying ipump with a gain of 25 implemented by several current mirror stages with a current short pulse generator.

The circuit implementation is shown in Fig. 5, where M1-M8 is a linearized transconductor [8] forming $k1 \times Vin$ with the four switches controlled by the SDM comparator ($Vout+$, $Vout-$) changing the output current polarity of the transconductor circuit. The transconductor is linearized by the feedback provided by M3 and M4, where the W/L ratio of M1 and M3 is chosen to be 6.6. The fixed current with a magnitude of $|k2 \times Vref|$ is the current that goes through the branch of M11 and M10. The current that goes through M12 in Fig. 5 is the summing current of the linearized transconductor circuit and the drain-source current of M11. The complete ipump reference current is mirrored to M13 and is amplified by the subsequent multiple current mirror stages and the stage of current pulse generator.

Next step, we need a pulsed current source that can generate sharp, clean current pulses of ns duration. This is achieved by a low impedance source follower, pulls up for the gate voltages of the actual current sources. When S6 is conducting, node Vb is grounded, no current flows in M24. Vgs22 of the source follower driver is large, but no current flows through M22 since S5 is open. When S6 is opened and S5 is closed, high current Ids22 (due to high Vgs22 = Va) flows through M22 and M23, charging node Vb very quickly to a correct gate bias for M24. When S5 starts to

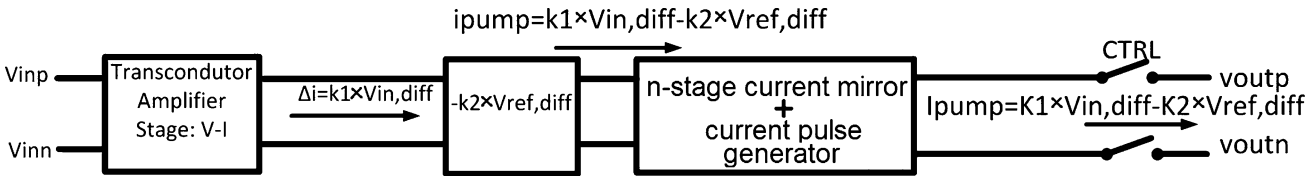



**Fig. 4** Block diagram of the current pumping circuit

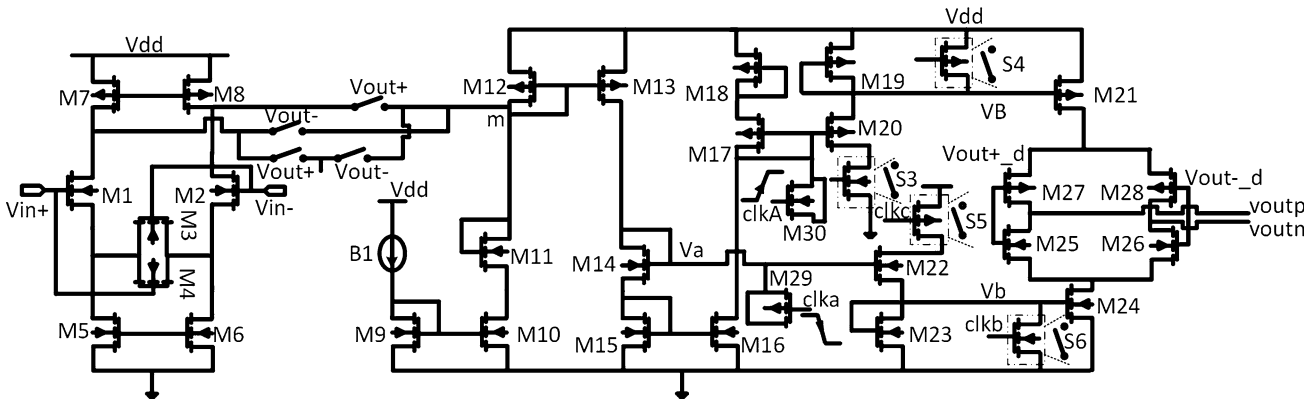



**Fig. 5** The schematic of fully differential current pumping circuit

conduct, the drain voltage Vd22 rises to Vdd rather quickly, pulls node Va upwards. This issue is minimized by dummy feedthrough via M29 to node Va. The time constant in node Vb need to be small to make sure that node Vb rises to the desired value very quick. Hence the channel length of M24, M23 has to be chosen as short as 200 nm. The current PMOS side works similarly, generates current source instead of sinking.

The current pump circuit is a compromise between the sharp/clean current pulse and precision. It was estimated that the injected charge can have error up to 20%, and still 50% of power savings in the OTA is obtained. Hence, the pumping circuit does not need to be extremely precise.

## 4 Simulation results of the pumping current with the fixed short pulse

A conventional second-order delayed cascaded 1-bit SC SDM was designed using generic 90-nm CMOS process with 1.2 V supply voltage. The input signal frequency fin is 48.8 kHz, sampling frequency fs is 50 MHz, and oversampling ratio is 128. The continuously controlled current pulse charge injection described in Chapter 3 was experimented and compared to a conventional design dimensioned for ten-bit performance.

Figure 6 is a simulation example of the transient response of the first integrator during the integration phase with the proposed current pumping method. Vi represents the transient behavior curve of the OTAs input during the whole integration phase (note that S5 which is controlled by clk5 is connected to the input of the OTA, aiming for isolating the OTA during the charge injection period), and the initial input voltage drops an order of magnitude to 44.34 mV. Vout is the output transient response of the first stage during the integration phase. Figure 7 is simulation results of the OTA initial input voltage step Vi0 vs. the input signal Vin, with and without the proposed current pumping method. The initial input voltage step is reduced from maximum of 600 to 58–59 mV, which makes the final settling much easier.

Figure 8 shows the simulated 65,536-point FFT output spectra obtained for both the conventional SDM (black solid line) with the original OTA and the proposed current pumping structure (grey dashed line) with the bias current reduced to 27.7% in the first stage OTA. The Spurious-Free Dynamic Range (SFDR) and the Signal-to-Noise and Distortion Ratio (SNDR) of the conventional structure are 69.8 and 65.6 dB, while the SFDR and the SNDR of the proposed continuously controlled current pumping structure are 70.2 and 66 dB. That is, the performance is the same as in the conventionally dimensioned SDM. Figure 9 shows the FFT output spectra with the OTA which decreases the current to 27.7% of the original current, but without the proposed current pumping circuit, resulting in SFDR and SNDR of 43.6 dB and 39.5 dB, it shows that the use of signal dependent current pumping improves SFDR by 69.8–43.6 = 26.2 dB, and improves SNDR by 65.6–39.5 = 26.1 dB, respectively.

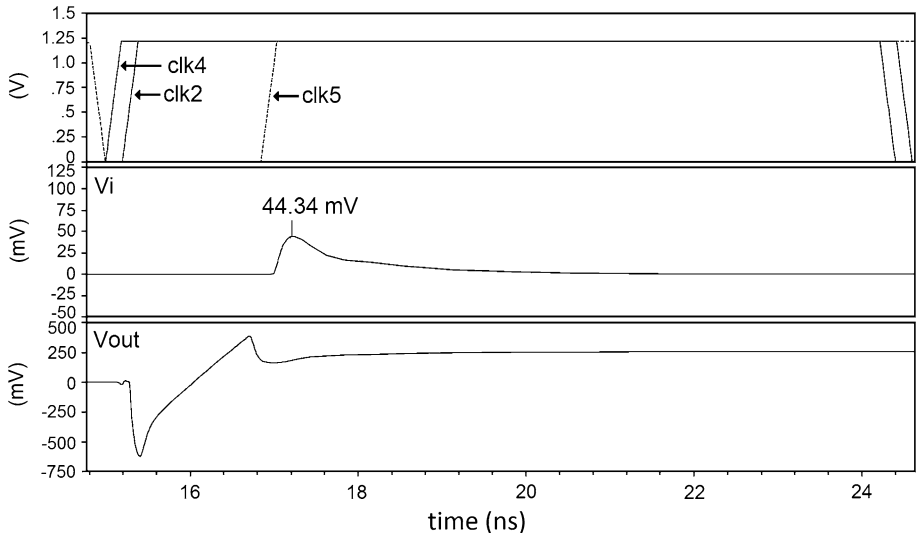



**Fig. 6** Simulated settling transient response of the integration phase

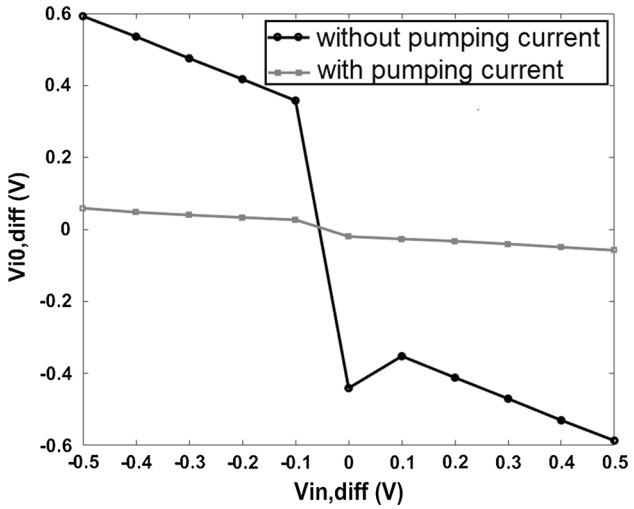



**Fig. 7** Initial input voltages comparison with/without the dynamically controlled current pumping circuit

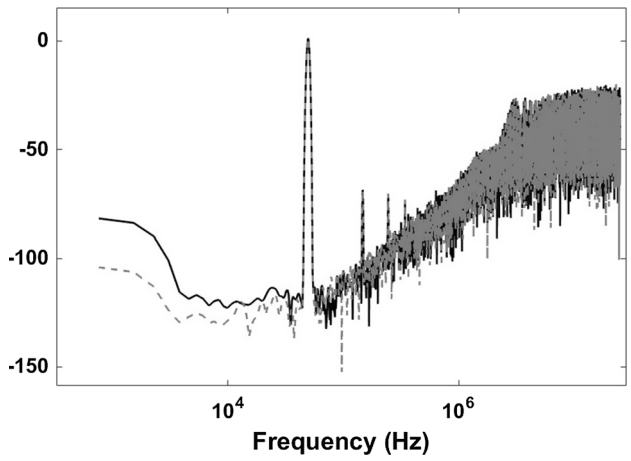



**Fig. 8** FFT spectrum of the conventional SDM without/with the current pumping circuit

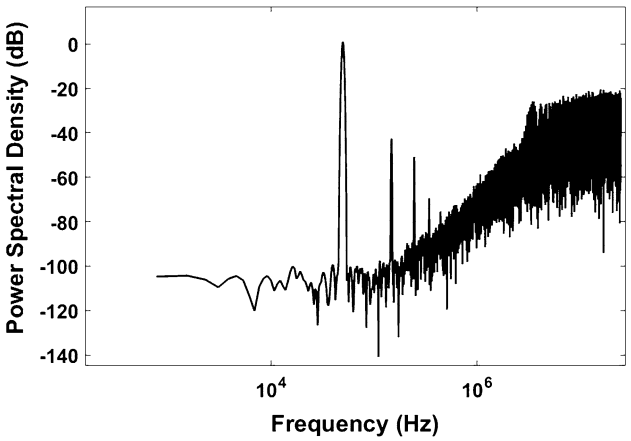



**Fig. 9** FFT spectrum of the conventional SDM with the relaxed OTA

Table 1 summarizes the performance and bias current of the single-stage folded cascaded OTAs that were designed for the conventional structure and for the proposed current pumping structure. The OTA of the first integrator is the dominant power consumer of the SDM, consuming 1140 μA in the conventional structure throughout the entire clock period (20 ns). The continuous current pumping circuit consists of the transconductor-amplifier (Gm-amplifier), the current mirror stages, the current pumping stage (IM23, IM19) and the output stage of current injection (IM24, IM21). The transconductor amplifier and the current mirror stages operate the entire clock period (20 ns) and consume 99.5 μA, but the high-current pumping stage (IM23, IM19) and the output stage of current injection (IM24, IM21) are on only during the short pumping period ($\Delta t = 1.4$ ns) and consume 357 μA over $\Delta t = 1.4$ ns. The total power consumption of the current pumping circuitry is 11% of the original first stage OTA. When current pumping is used, the bias of the first stage

**Table 1** OTA performance comparison

| | Original main OTA Without CP | Relaxed main OTA With CP | Current pumping (CP) circuit | |
|---|---|---|---|---|
| OTA structure | One stage folded cascade OTA | One stage folded cascode OTA | Gm-amp with CM stages | (CP + output) stages |
| Phase margin | 70.8° | 74° | – | |
| Gain | 66.5 dB | 60.29 dB | – | |
| Unit gain bandwidth | 331.7 MHz | 164.4 MHz | – | |
| Slew rate | 338 V/μs | 93.5 V/μs | – | |
| Total current (working period) | 1140 μA (20 ns) | 316 μA (20 ns) | 99.5 μA (20 ns) | 357 μA (1.4 ns) |
| Power consumption (%) | 100% | 27.7% of the original first stage OTA | 11 % of the original first stage OTA | |

OTA is reduced to 316 μA, which is 27.7% of the original OTA. Considering the power dissipation overhead by the current pumping circuit, the first integrator with the current pumping circuit reduces the first stage power by 60% compared to the conventional structure, providing approximately 43% power reduction for the whole SDM.

## 5 The circuit implementation of the three-level pumping current

The three-level pumping current circuit consists of a simple dynamic 1.5-bit ADC, three switchable pumping current sources that represent the charge injection of three separate levels, and logic gates to generate the control signals for the pumping current sources. The dynamic ADC consists of two parallel voltage comparators that directly sense and compare the input voltage to the corresponding threshold voltages $|\ VinFS/6\ |$ and $-|\ VinFS/6\ |$, where VinFS is the full scale input range.

The operation of the simple dynamic ADC in Fig. 10 is straightforward: the comparision results in a thermometer code (Di+ Di−) which is encoded into controls X1 X2 X3 by logic gate.

- X1 represents the input voltage during the low voltage range of $[-|\ VinFS/2\ |, -|\ VinFS/6\ |]$,
- X2 representing when the input voltage is in the middle range, and
- X3 at logic one represents when the input voltage is in the high voltage range of $[|\ VinFS/6\ |, |\ VinFS/2\ |]$

## 6 Simulation results of the three-level pumping current

The same second-order delayed cascaded 1-bit SC SDM was simulated again. Figure 11 shows an example of the transient response of the first integrator during the integration phase. Vi of Fig. 11 (middle curve) represents the transient behavior curve of the OTAs input during the whole integration phase. After the current pumping circuit stops, the initial input voltage drops to − 65 mV which avoids the slew rate region, and then directly enters the linear settling region. The peak initial input voltage of the OTA is reduced by a decade as compared to the 600 mV in the conventional structure. Figure 12 indicates that the initial input voltage of the OTA are significantly reduced within [−65 mV, 65 mV] compared to the initial input voltages in the conventional structure.

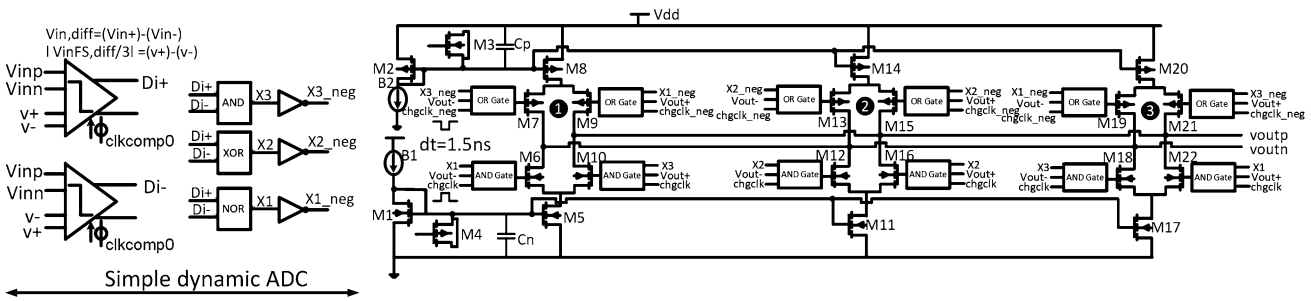



**Fig. 10** The schematic of the three-level current pumping circuit

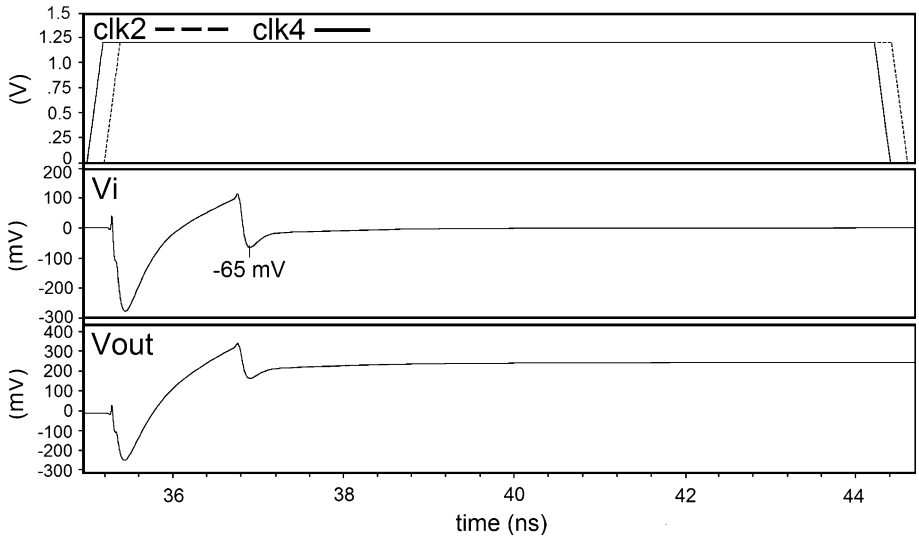



**Fig. 11** Simulated settling transient response of the integration phase

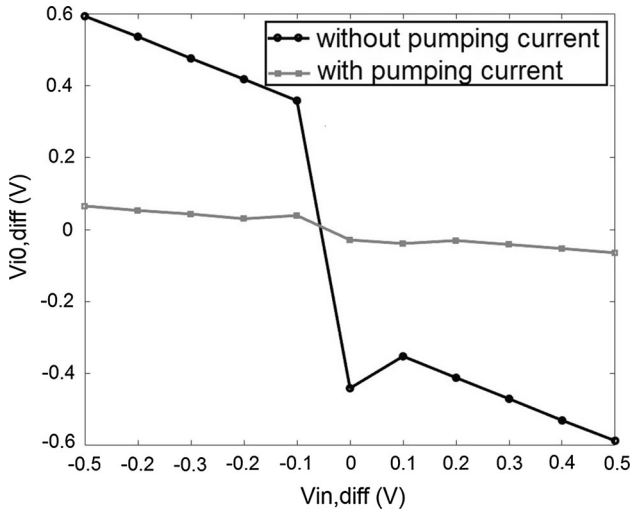



**Fig. 12** Initial input voltages comparison with/without the logic-controlled three-level current pumping circuit

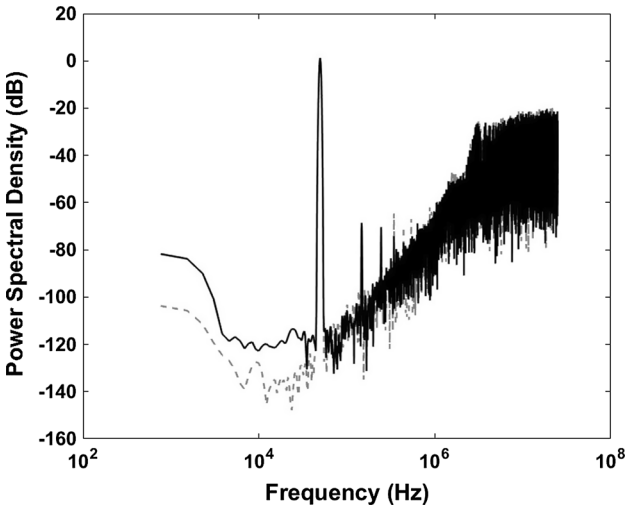



**Fig. 13** The FFT spectrum of the conventional SDM without/with the three-level current pumping circuit

Figure 13 shows the simulated 65,536-point FFT output spectra for the conventional SDM with the original OTA (black solid line) and the proposed three-level pumping current technique with the relaxed OTA in the first stage (grey dashed line). The SFDR and SNDR of the original structure are 69.8 dB and 65.6 dB respectively, while the SFDR and SNDR of the three-level pumping current technique are 70.4 dB and 66.2 dB respectively. Figure 14 shows the FFT output spectra with the relaxed OTA of the first stage but without the proposed current pumping circuit, resulting in SFDR and SNDR of 52.7 dB and 48.6 dB. Therefore it shows that the three-level logic pumping current method gave about 17 dB improvement both in SFDR and SNDR.

Table 2 summarizes the characteristics of the OTAs used in the setup. The dominant power dissipation of the proposed current pumping circuit is the three current source branches and the parallel comparators working in the comparison mode. The comparators consume 85.5 μA in the comparison mode. One of the three current source branches is chosen in every current pumping period, giving on average 257.4 μA (including bias currents) for Charge pumping mode. When the current pumping mode is off, the comparators are in the reset mode, all the three current source branches are switched off. The current of the three current source branches (including bias currents) in the non charge pumping mode is about 19.4 μA. Including digital logic gates and comparators, the total charge is about 19.7 μA during the non charge pumping mode. The relaxed OTA of the first integrator with the current pumping circuit uses 440 μA for the entire clock period. The total power consumption of the current pumping circuit is 4.3% of the

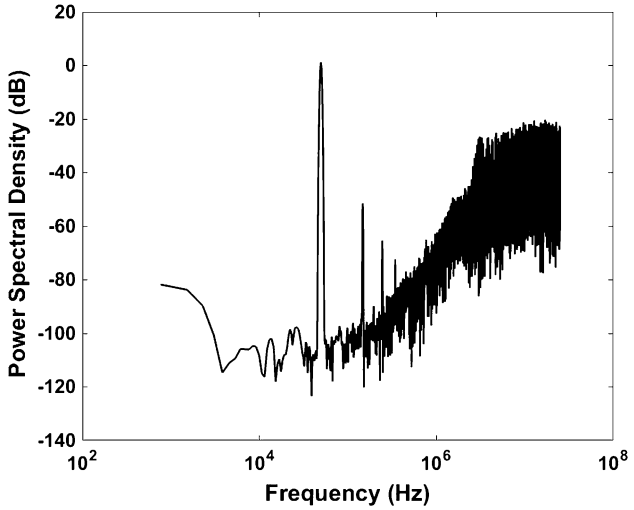



**Fig. 14** The FFT spectrum of the conventional SDM with the relaxed OTA

original OTA, and the bias of the OTA can be reduced to 38.6% of original.

Considering the power dissipation overhead by the proposed current pumping circuit, the first integrator with the current pumping circuit reduces the first stage power by 56% compared with the conventional structure, provides an approximately 40% power saving for the overall SDM with no loss in performance. Figure 15 summarizes the power consumption for the two proposed current pumping methods. The power consumption of the relaxed first OTA using 3-level pumping current is larger compared to the relaxed first OTA using dynamic continuously controlled pumping current, but the circuit of the 3-level pumping current requires less than half the current of the continuously controlled pumping current circuit. Therefore, both proposed methods can save about 40% of the original power consumption.

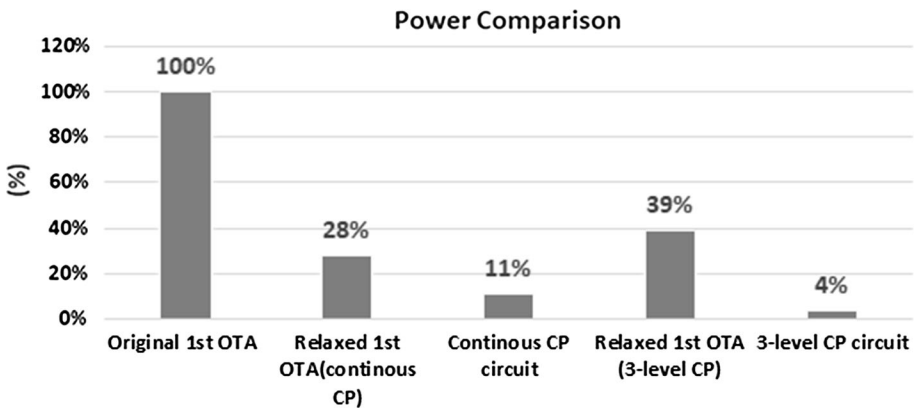
## 7 Conclusion

Two methods of open-loop charge injection at the output of the first integrator were studied to reduce the power consumption of a SC integrator. The main idea is to use capacitive charge sharing principle to feed an approximate amount of pre-calculated charge Qpre to the output of the OTA at the start of the integrator period, minimize the initial transient voltage in the input of the first amplifier and hence bypass the slewing of the amplifier. Neither of the methods needs to be very precise, as the purpose is just

**Table 2** OTA performance camparison

| | Original OTA no CP | Relaxed OTA with CP | Current pumping (CP) circuit | |
|---|---|---|---|---|
| OTA structure | One stage folded cascade OTA | | Three-level CP circuit | |
| Phase margin | 70.82° | 74° | – | |
| Gain | 66.5 dB | 61.3 dB | – | |
| Unit gain bandwidth | 331.7 MHz | 185 MHz | – | |
| Slew rate | 338 V/μs | 131 V/μs | – | |
| Total current | 1140 μA | 440 μA | CP branches | |
| | | | 257.4 μA CP mode (M) | 19.4 μA non-CP M |
| | | | Comps | |
| | | | 85.5 μA comp M | 761 pA reset M |
| Power consumption (%) | 100% | 38.6% of original 1st stage OTA | 4.3% of original 1st stage OTA | |

**Fig. 15** Power comparison



for an order of magnitude cancellation. Also, neither of the methods adds any capacitive loading to the output of the integrator during the integration phase. Considering the power dissipation overhead by the two active charge pumping methods, the first integrator with the two proposed charge pumping techniques respectively reduce the first stage power by 60% and 56% compared to the conventional structure. This is higher than the 43% saving reported for dynamic biasing of OTA in [5]. Circuit simulations of the two proposed methods show that a 10-bit performance can be obtained requiring only 60% power dissipation of a traditional structure without proposed techniques.

The circuit has not been implemented, so the practicality of the approach needs to be discussed. It is true that the charge balance depends on the parasitic and processing conditions, but yet the charge equations consist of relatively large charge in the sampling and integrating capacitors. Moreover, 10–20% error in the injection still allows bypassing the slewing region, making power savings possible. Hence, the multilevel coarse cancellation is rather robust and cost-effective to implement. In the continuously operating canceller the most critical part is the current pump circuit, where both the output impedance of the current sources and the time constants inside the pulser affect the amount of injected charge. Thus, this requires a factory gain calibration, which can be implemented either by adjusting the bias current of the pump, or by adjusting the on-time of the pulsing circuit.

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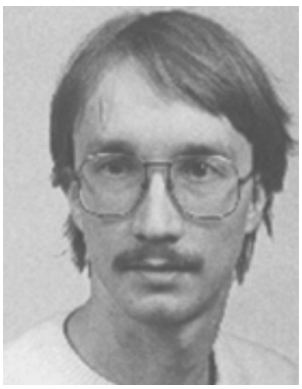

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