Ka-Band 3-Stack Power Amplifier with 18.8 dBm P_{sat} and 23.4 % PAE Using 22nm CMOS FDSOI Technology

Janne P. Aikio, Mikko Hietanen, Nuutti Tervo, Timo Rahkonen, Aarno Pärssinen

University of Oulu, Department of Information Technology and Electrical Engineering
Oulu, 90014, Finland

***Abstract*— This paper presents a fully integrated, three-stack power amplifier for 5G wireless systems, designed and fabricated using 22 nm CMOS FDSOI technology. The frequency of operation is from 25 GHz to 30.5 GHz, with a maximum 3 dB bandwidth of 5.5 GHz and a maximum gain of 9.9 dB. Maximum RF output power, power-added efficiency (PAE) and output 1 dB compression point are 18.8 dBm, 23.4 % and 14.9 dBm, respectively, achieved at 28.5 GHz.**

***Index Terms*— CMOS, SOI, RF, mm-Wave, stacked power amplifier, PA, wireless communications, 5G.**

I. Introduction

To achieve higher data rates envisioned by the fifth generation (5G) of wireless systems, wideband systems operating at millimeter wave (mm-Wave) frequencies are required [1]. In addition, massive parallelism in the form of massive multiple-input multiple-output (MIMO) systems and phased arrays are proposed [2], [3], [4].

In large phased arrays, the output power levels required at each antenna decrease proportionally to the number of antennas. It is evident that in such phased arrays each antenna is preceded by a medium power amplifier (PA) preferably integrated in the transceiver RFIC.

In this paper, we describe a three stack PA at 28 GHz implemented using Global Foundries 22 nm CMOS FDSOI technology. 22FDX is fully depleted CMOS technology providing e.g. fT and fMAX for nFET device up to the 347 GHz and 371 GHz, respectively [2]. The nominal VDD of the 22nm FDSOI is only 0.8 V limiting the achievable voltage swing at the output of the PA considerably. However, the FDSOI technology enables transistor stacking and hence allows increasing the operating voltages.

II. Stacked Power Amplifier

The schematic of the designed stacked PA is shown in Fig. 1. The target center frequency was 28 GHz and to achieve that the input match was designed using two resonators, i.e. parallel L_1 and C_1 and center tapped L_2 and C_2. The frequency response of the PA is determined mainly by the input resonators allowing wideband output match to 50 Ω. The width of the transistors M_1 - M_3 is 300 µm and gate of M_1 is predominantly capacitive. Second input resonator is resonating out this capacitive part providing good 50 Ω input match. Since the resistive parasitics of the L_2 has a significant impact on the Q factor of the resonator, by taking the signal out from the center tap of the L_2, the sensitivity to the resistive parasitics is reduced to a large extent.

Due to the low VDD the transistors need to be stacked in order to increase the achievable signal swing at the output node. By stacking 3 transistors we are able to increase the VDD from nominal 0.8 V up to 2.8 V, which provides output power close to 19 dBm.

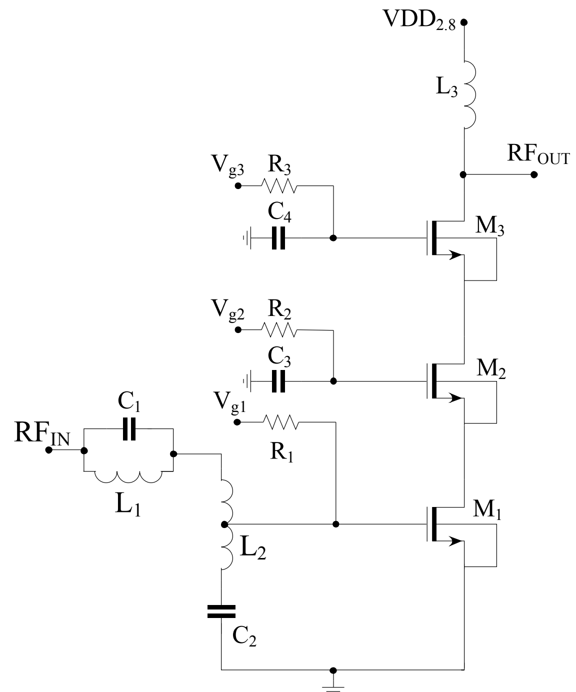

Fig. 1. Schematic of the Stacked PA.

The gates of the transistors in the stacked structure are not RF grounded but the gate impedances using C_1 and C_2 are dimensioned to control the inter-stage matching and voltage swing in the source nodes of M_2 and M_3. Keeping the source waveforms synchronous and progressively increasing is essential in terms of avoiding breakdown. In addition, device size and gate capacitances are optimized

for direct $50\,\Omega$ output load. Each gate has a separate bias control allowing the bias optimization for maximum power and efficiency. Nominal bias point is in class AB.

III. Measurement Setup

The micrograph of the developed integrated circuit (IC) is shown in Fig. 2. The dimensions of the PA, including the input and output pads is $550\,\mu\mathrm{m} \times 380\,\mu\mathrm{m}$. The active area without pads is $294\,\mu\mathrm{m} \times 380\,\mu\mathrm{m} = 0.11\,\mathrm{mm}^2$.

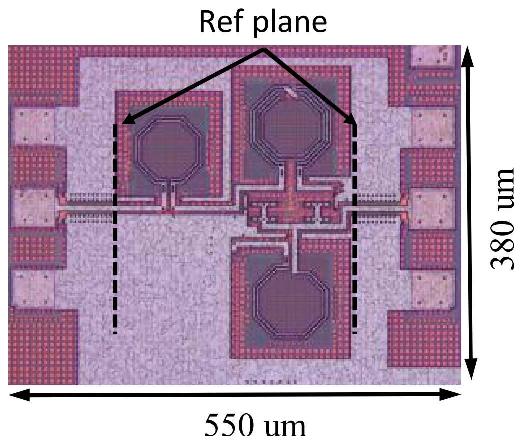

Fig. 2. Chip photograph of the fabricated PA.

The PA was measured using PNA-X network analyzer with Cascade Infinity I40 probes. As it can be noted from Fig. 1, there are no coupling capacitors on-chip, and therefore external bias-Ts (Keysight 11612B) were used to measure the actual bias voltages and block the DC from the network analyzer.

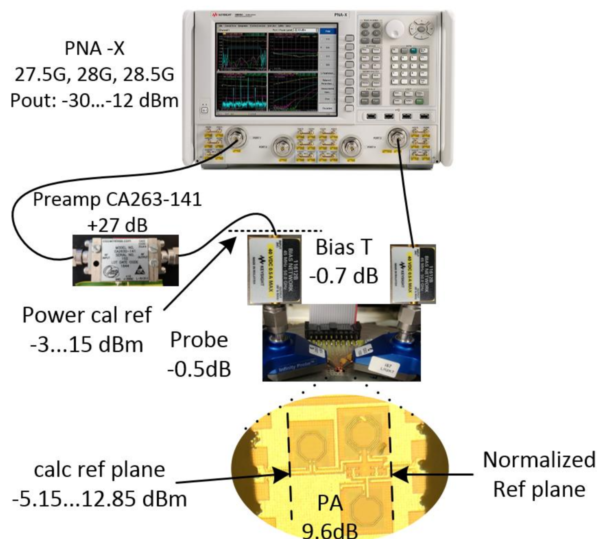

Fig. 3. Measurement setup for 1-tone large signal probe measurements using network analyzer.

Complete TRL calibration standards were designed and fabricated on-chip enabling full 2-port S-parameter measurements. For large-signal measurements additional pre-amplifier (Caio Wireless CA263-141) was used due to the fact that the PNA max output power was not enough to drive the PA into the compression. The measurement setup for large signal measurements is shown in Fig. 3 The power calibration was performed at the end of the cable before the Bias-T that was directly connected to the probe. The measurement was normalized using the on-chip Thru standard. The losses of the bias-Ts, connectors, probe and the Thru were measured and hence the actual input amplitude of the PA was calculated to the edge of the active PA (see reference planes in Fig. 2 and Fig. 3).

IV. Experimental Results

The measured S-parameters are shown in Fig. 4. It can seen that the peak gain 9.9 dB occurs at $28.5\,\mathrm{GHz}$. The 3dB bandwidth is from $25\,\mathrm{GHz}$ to $30.5\,\mathrm{GHz}$ matching 3GPP/NR FR2 band n257 [1]. The input and output matching at $28\,\mathrm{GHz}$ are -8.5 dB and -6.5 dB, respectively. The drain of the M_3 is directly connected to the output and thus S22 is mainly determined by the bias feed L_3 but also affected by the gate capacitors and input resonators. As a result the output matching is a compromise of decent match and good large signal performance.

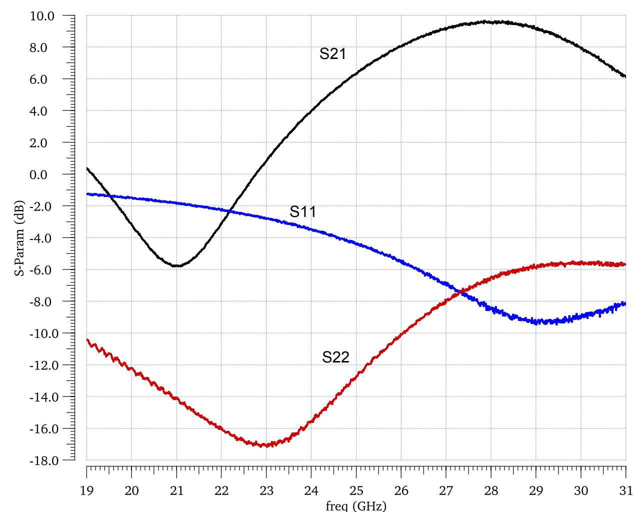

Fig. 4. Measured S-parameters of the stacked power amplifier.

Results of the large signal measurements at $28.5\,\mathrm{GHz}$ are shown in Fig. 5. The measured 1dB compression point and P_{sat} were $14.9\,\mathrm{dBm}$ and $18.8\,\mathrm{dBm}$, respectively. The max PAE ($23.4\,\%$) occurs at 3dB compression point ($18.2\,\mathrm{dBm}$) with P_{DC} as low as $176\,\mathrm{mW}$. The PAE at 1dB compression point is 16.8 % (see also Fig. 6 b)) and $9\,\mathrm{dB}$ back-off from P_{sat} (typical PAR of OFDM signal) the PAE is $12\,\%$ with P_{DC} of $141\,\mathrm{mW}$. Total AM-PM is less than 10°, which indicates relatively linear performance.

Measured compression, PAE and AM-PM as a function of frequency around 28 GHz is shown in Fig. 6 a), b) and c), respectively. It can be seen that the 1dB and 2dB compression points are higher at 28 GHz. However, 3dB compression and P_{sat} are higher at 28.5 GHz. Similar trend can be seen in PAE curves in Fig. 6 b). On the other hand, the AM-PM in Fig. 6 c) shows the most linear performance at 28 GHz in each curve.

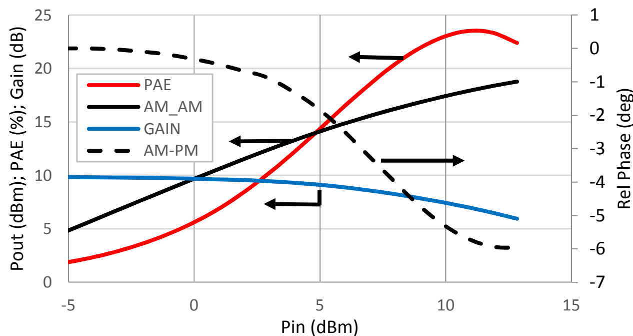

Fig. 5. Measured PAE, AM-AM and AM-PM at 28.5 GHz.

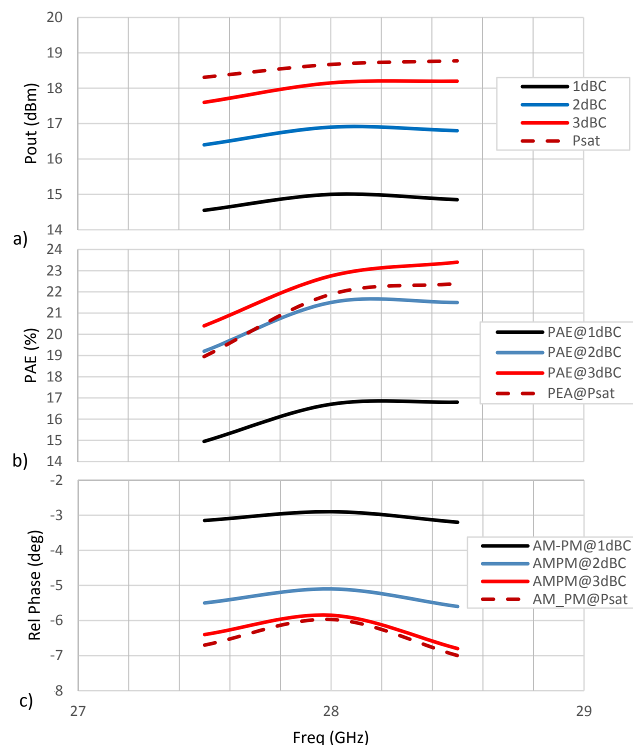

Fig. 6. Measured, a) compression, b) PAE and c) AM-PM vs. frequency.

A summary of the key performance parameters against the recent comparable state-of-the-art stacked PAs is shown in Table I. It can be seen that the achieved power is competently placed. The proposed PA has the smallest active area, hence giving the best output power relative to used area. Along with [2] the proposed stacked PA is one of the first reported using 22nm CMOS SOI technology.

TABLE I
CMOS POWER AMPLIFIER PERFORMANCE SUMMARY.

	This work	[2]	[3]	[4]
Tech.	22 nm CMOS SOI	22 nm CMOS SOI	45 nm CMOS SOI	28 nm CMOS
Topology	3-stack	Diff. 3-stack	2-stack	Diff. 2-stack
Frequency (GHz)	25–30.5	28	25–32.3	26.5–29.5
P_{1dB} (dBm)	14.9 @ 28.5 GHz	-	17.6 @ 26.7 GHz	18.6 @ 28 GHz
P_{sat} (dBm)	18.8 @ 28.5 GHz	21 @ 28 GHz	18.9 @ 26.7 GHz	19.8 @ 28 GHz
Peak PAE(%)	23.4 @ 28.5 GHz	30 @ 28 GHz	40.5 @ 26.7 GHz	41.4 @ 28 GHz
VDD (V)	2.8	-	2.4	-
Active area (mm^2)	0.11	-	0.18	0.28

V. CONCLUSION

In this work we demonstrated a fully integrated three stack power amplifier targeted toward future communication system using 22nm CMOS SOI technology. It was shown that the PA can operate over a frequency range of 25 GHz–30.5 GHz. The PA achieved a maximum saturated power of $18.8\,\mathrm{dBm}$ along with a maximum peak PAE of $23.5\,\%$ and the output 1 dB compression point of $14.9\,\mathrm{dBm}$ at 28.5 GHz. DC power consumption at 1 dB compression point and at saturated output power levels were $176\,\mathrm{mW}$ and $196\,\mathrm{mW}$, respectively. The active area is as small as $0.11\,\mathrm{mm}^2$.

ACKNOWLEDGMENT

This research has been financially supported by the Nokia Corporation Ltd and Academy of Finland 6Genesis Flagship (grant 318927). The authors would also like to acknowledge Global Foundries for the silicon processing and technical support.

REFERENCES

[1] 3GPP, "Base Station (BS) radio transmission and reception," 3rd Generation Partnership Project (3GPP), Technical Specification (TS) 38.104, 09 2018, version 15.3.0. [Online]. Available: http://www.3gpp.org/ftp/Specs/archive/38_series/38.104/38104-f30.zip

[2] S. N. Ong *et al.*, "A 22nm FDSOI Technology Optimized for RF/mmWave Applications," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2018, pp. 72–75.

[3] N. Rostomyan, M. Ozen, and P. Asbeck, "Comparison of pMOS and nMOS 28 GHz high efficiency linear power amplifiers in 45 nm CMOS SOI," in *2018 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Jan 2018, pp. 26–28.

[4] B. Kim *et al.*, "Linear PA at mm-Wave band for 5G application," in *2017 10th Global Symposium on Millimeter-Waves*, May 2017, pp. 80–82.