Yield and Electrical Functionality of the Glass Laminated Conductive Wires and Connectors

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Abstract—**Large area electronics is becoming an embedded part of structural elements such as automotive and architectural glasses. In this study, the effect of glass lamination based fabrication process on the electrical performance and production throughput yield (TPY) of printed conductive wires and surface mounted (SMD) connectors on polyethylene terephthalate (PET) carrier film were investigated by measuring their electrical conductivity after lamination. Based on the experiments, lamination decreases the production yield of conductive wires and connectors due broken wires or dislocated connectors, especially if they are located close to the corners of laminate. On the other hand, lamination was observed to improve the electrical conductivity of wires. In addition, some potential failure mechanisms are discussed.**

Index Terms—**Electronics manufacturing, Large area electronics, Production yield, Structural Electronics**

I. INTRODUCTION

THE recent development in the field of material and manufacturing technology has enabled completely new means for manufacturing processes of electronics [1-3]. Printing techniques that have already existed since printing revolution in the 1440's Germany [1] have recently been found as a very promising method to fabricate thin, flexible and deformable large area electronics [1-4]. Printed electronics offers many benefits over more traditional, silicon-based rigid electronics. Manufacturing printed electronics additively induces less waste material, making it more environmentally friendly and inexpensive manufacturing method. As a manufacturing method, it is also applicable to fabricate electronics in a large volume rates efficiently, which allows manufacturing large-area and lightweight devices such as paper-thin displays, which require a large number of components [1-5]. Printed electronics does not completely replace silicon-based electronics, however, it opens new possibilities for disposable low-cost electric applications such as printed organic light emitting diodes (OLEDs) used in display technologies or organic photovoltaic cells (OPVs) used in photovoltaic energy harvesting [1, 6-7]. As part of the development, implementation of electronics inside of glass-laminate structures as embedded components has become reality. This has become considerable application for the productions in the field of automotive and architecture industry.

Integration of printed electronics inside the laminated glass utilizes the latest know-how of materials and manufacturing technologies. In this approach, electronics' components are not only covered by glass, but they are embedded as a solid part of the glass laminate, making it different from the conventionally glass protected devices such as solar panels or displays. Embedding components as solid part of the laminate is beneficial as the laminate offers protection against mechanical stresses by dividing mechanical forces into larger areas [8]. Another benefit from glass lamination is improved thermal conductivity due higher heat transfer coefficient of intermediate material [9]. Maturity level of the technology is relatively low and thus the knowledge about the optimal materials, manufacturing parameters and their influence on production yield, quality, products' lifetime and performance are limited. In order to get better understanding of influence of the lamination on printed electronics and to find reasons for systematic failures and to evaluate throughput yield, an electrical functionality test is reguired for glass laminated electronics. It is also worth mentioning that this know-how helps to optimize and develop the mass-manufacturing technologies for these types of products.

Reliability analysis of printed electronics has been intensively conducted over the past years [10-16] but similar analysis for glass laminated printed electronics has just initiated [17]. Previous published results focus on the aspects relevant to surface mounted LED on plastic carrier film. Those experiments show that lamination causes significant thermomechanical stress to laminated electronics and thus has an influence on the electronics properties and production yield. In this study, the electronics testing experiments were done to understand the influence of the lamination on the electrical characteristics of printed conductive wires (with and without surface mounted connectors) and to the production yield of them.

II. MATERIALS AND METHODS

Experimental verification and analysis were performed for ten identically processed glass laminates with ten different conductive wire patterns to obtain reasonable number of statistical data for valid yield analysis. In addition, two different

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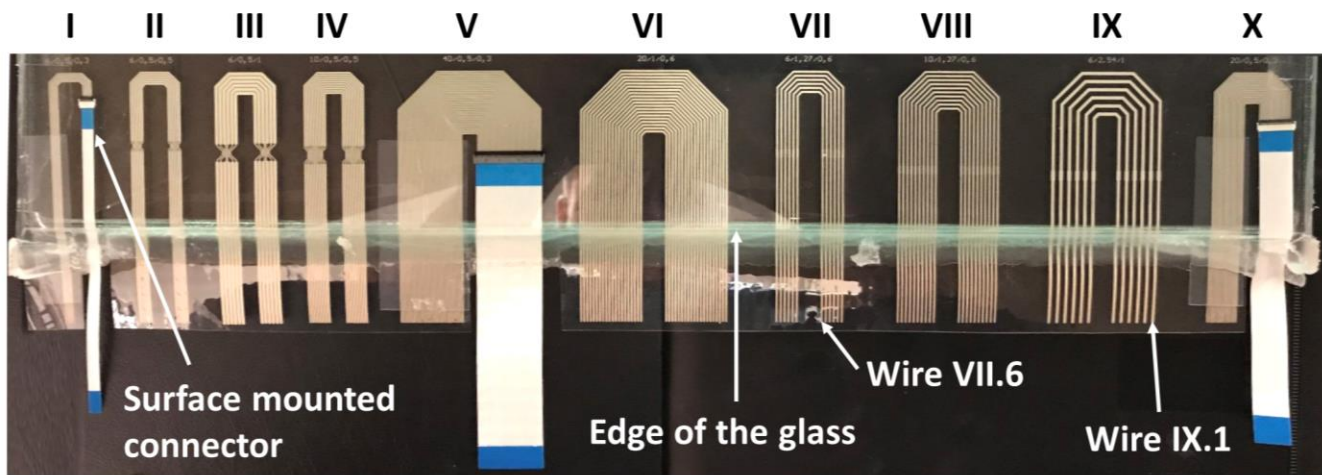
Fig. 1. Representative photography of the laminated test structure (samples of A1-A10). The conductive pattern layout of the samples B1 and B2 is identical but they are not laminated. All laminates have 10 conductive wire patterns (I-X) with surface mounted connectors on patterns I,V and X. In order to get galvanic contact to the conductors, the part of the PET is outside the laminate. Each conductive wire is identified with a number (for example VII.6 or IX.1).

variants of the test samples were analyzed as a reference. The more detailed features of these samples are described in this chapter.

A. Specifications of the used materials

Three different variants of laminated test samples with same conductive wire pattern were fabricated and analyzed. Type 1 samples are laminated in glass containing screen printed conductive wires with 10 different patterns on PET and surface mounted connectors (A1-A10). Type 2 samples are used as a reference for the laminated samples. They are equal with the sample type 1, but they are not laminated (B1). Type 3 samples are equal to sample type 2 with an exception that it does not have surface mounted connectors (B2). These reference samples are used to distinguish the influence of the connectors on the electrical characteristics of the laminates (see Fig. 1). Technical details of the used materials are summarized in Table I.

B. Layout of the test patterns

The layout of the test pattern was designed to investigate the effect of physical dimensions of the wires on the production yield. In addition, three surface mounted connectors were added on PET before lamination to get yield data of connectors with standardized interfaces.

All the tested samples (A1-A10 and B1-B2) were based on same conductive wire design. Each sample contained 10 silver trace patterns (I-X) with different pitch (0.5, 1.0, 1.27 and 2.54 mm) and line width (0.3, 0.5, 0.6 and 1.0 mm). The number of conductive wires varied between 6-40 wires. The key technical parameters of each pattern is shown in Table II and the photograph of laminated test structure is shown in Fig. 1.

C. Fabrication process of laminated electronics

In this concept, laminate fabrication process has three main phases: 1) Printing of the conductive wires, 2) Assembling and bonding discrete connectors on substrate and 3) Laminating the film into the glass. The used materials are summarized in Table I.

Conductive wires were rotary screen printed on flexible plastic substrate (PET, thickness 125 µm) in a roll-to-roll (R2R) process with proper heating based post-treatment. After the printing, three different type of connectors were assembled and bonded with wires on top of the PET. Before the bonding, the roll with conductive wires were cut to the sheets including ten different patterns shown in Fig. 1. First bonds of the connectors were done with UV-curable support epoxy, which prevents the connectors from moving and possibly breaking the isotropically conductive adhesive (ICA) bond and causing i.e. a short-circuit. Second, conductive bond was done by dispensing an ICA adhesive on the pins of the connectors. ICA is heat cured after assembling. Before laminating the PET, an additional smaller

TABLE I
SPECIFICATIONS OF USED MATERIALS AND COMPONENTS

Material/Component	Details	Comment
Conductive adhesive	Epotek H20E	Isotropically conductive adhesive
Conductive wires	Asahi LS-411AW	Silver paste for screen printing
Connectors	Series: WR-FCC (Würth Electronics)	Three variants: 6, 20 and 40 connections
Foil	Polyethylene terephthalate (PET)	Carrier film for electronics
Intermediate material	Polyvinyl butyral (PVB)	Adhesive for glass lamination
Glass	Silica glass	
Support epoxy	Loctite AA 3525	Supporting epoxy

TABLE II
PATTERN IDENTIFICATION AND DIMENSIONAL PARAMETERS

Pattern	Number of wires	Pitch	Width of wire
I	6	0.5 mm	0.3 mm
II	6	0.5 mm	0.5 mm
III	6	0.5 mm	1.0 mm
IV	10	0.5 mm	0.5 mm
V	40	0.5 mm	0.3 mm
VI	20	1.0 mm	0.6 mm
VII	6	1.27 mm	0.6 mm
VIII	10	1.27 mm	0.6 mm
IX	6	2.54 mm	1.0 mm
X	20	0.5 mm	0.3 mm

TABLE III
PATTERN SPECIFIC PRODUCTION YIELD OF LAMINATED CONDUCTORS AND CONNECTORS

ID	I	II	III	IV	V	VI	VII	VIII	IX	X
A1	100%	100%	100%	70%	83%	100%	100%	100%	100%	70%
A2	100%	33%	100%	100%	93%	100%	100%	90%	100%	90%
A3	67%	50%	0%	10%	53%	0%	0%	10%	83%	0%
A4	67%	50%	100%	100%	100%	95%	100%	100%	100%	0%
A5	83%	67%	100%	100%	93%	100%	100%	100%	100%	90%
A6	100%	83%	100%	90%	98%	100%	100%	90%	100%	65%
A7	100%	83%	100%	100%	98%	100%	100%	100%	100%	40%
A8	100%	67%	100%	80%	78%	90%	100%	100%	100%	10%
A9	33%	83%	100%	80%	8%	15%	100%	80%	100%	40%
A10	33%	67%	100%	100%	90%	100%	83%	90%	100%	75%

piece of PET was added on top of the conductors for samples I, V and X to prevent any damage on them during the lamination at the edge of the glass. Each sheet was laminated inside the glass utilizing PVB lamination process. In the lamination, the PET was assembled between PVB and glass sheets. De-airing of the laminate stack is done through silicon tube and then baked in autoclave in gradually increased temperature (~130 ^{0}C) and pressure (up to 9 bar). Laminates were cooled down to the ambient temperature before actual yield testing.

D. Number of samples and their identification

In total, ten glass laminates (A1-A10) were measured as test sample while only one piece of each reference samples (B1 and B2) were characterized. Each sample had 10 different conductive wire patterns identified with roman numbers I-X (See Fig. 1). The pattern identification with dimensional parameters of patterns are summarized in the Table II.

The patterns II-IV have also section in which the width and pitch of the conductors are narrowed. These dimensions are matching with the dimensions relevant to commonly used surface mounted components such as LEDs and regulators etc. thus, the resistance characteristics of conductors in pattern III is not directly comparable with the conductive wire with same lengths in pattern IX even though their cross-sectional area (defining the resistance) equals.

E. Resistance measurements

The resistance of each conductive wire in all patterns and sample types were measured 4 times to minimize the errors caused by the manual measurement. Digital multimeter devices (Mastech MS 8229 and Fluke 70 III) were used in these experiments. Galvanic contact of the multimeter probes to conductors were achieved on the edge of the PET film, which is remaining outside the laminate.

F. Optical coherence tomography measurements

Non-destructive structural characterization method, so called optical coherence tomography (OCT) was used in this study to evaluate structural changes caused by lamination and find reasons for the observed features of laminated electronics. OCT is widely used in (bio)medical measurements [18-19] but the same technology has been utilized also in industrial applications [17, 20-27] including the electronics quality inspection and reliability analysis [17, 22]. Briefly described, OCT is a light-based imaging method in which backscattered intensity profiles are recorded and typically, by lateral scanning

of a probing beam cross-sectional images are composed. The lateral and the axial (depth) resolutions of the used OCT (Hyperion, Thorlabs Inc.) are 8 µm and 5.8 (in air) respectively.

G. Profilometer measurements

Surface topology measurements of printed conductive wires were performed to determine cross-sectional area of printed patterns and to evaluate the printing quality. Optical profilometer (Bruker Contour GT-K0) was used in this study.

H. Pareto analysis

Pareto analysis, also known as 80/20 method, is a statistical tool for quality management to identify relations between causes and their effects on results. The basic principle of the method is that 20 % of all causes explains 80 % of all results. Benefit of Pareto analysis is to identify causes that have the most impact. When most impactful cause has been identified, it can be modified to improve the results [28-29]. In this study, Pareto analysis was utilized to understand and identify the causes for catastrophic failure in printed conductors.

III. MEASUREMENT RESULTS

A. Functionality after lamination

The production yield for the test samples (A1-A10) were analysed utilizing yield analysis by measuring the resistance of the printed wires of each pattern after lamination. The resistance values of non-laminated samples (B1 and B2) were
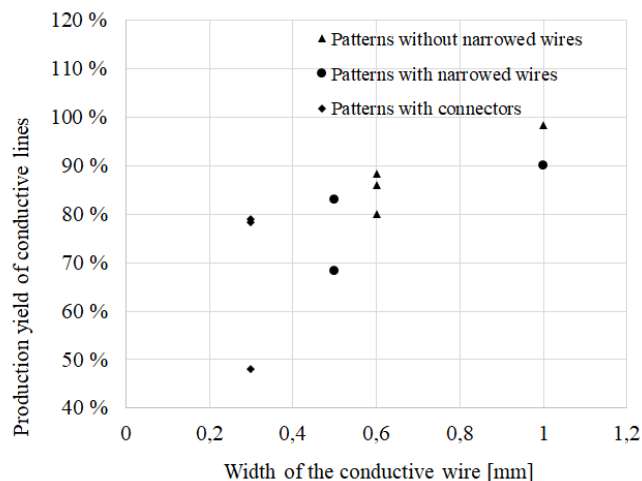
Fig. 2. The effect of line width on the production yield of conductive wires after lamination. The increased width improves the yield.

used as reference. The failure criteria of conductive wire was set so that if the absolute value of measured resistance had increased more than 100% from the initial resistance value (which depends on the physical measures of wires), it is considered as failed. The yield analysis was defined pattern by pattern (I-X) for each printed wire and obtained results are summarized in Table III.

Except the sample A3, which had very low yield (expected to be random fail), the production yield characteristics for laminated wires were coherent (sample A3 looks good in visual inspection). In case failure of the conductor was detected, the resistance was over the measurement range of used multimeter device. This type of phenomenon is referred as a catastrophic failure in electronics yield analysis. Excluding the laminate A3 from the analysis, patterns III and IX had 100 % yield which is crucial in industrial scale production of these type of laminated electronics.

The Fig. 2. shows that the production yield of printed conductors decreases when the width is decreasing. In case the width is 1.0 mm, the yield was found to be almost 100 % while the values for narrower wires were below 90 %. However, it is worth mentioning, that all showed yield values for each pattern are not fully comparable because their pitches are not equal, location in laminate differ and the number of wires is different. For example, the lower yield of patterns with surface mounted connectors (I, V and X) can be partially explained by their narrow width (0.3 mm).

The location of the pattern in the laminate have influence on the production yield. Once the pattern is too close to the corners of the laminate (I and X), the yield of functional wires is reduced. However, those patterns in the corner have surface mounted connectors (narrow line width), and thus unambiguous conclusions about the effect of location on production yield requires further verification.

B. Relative resistance changes of laminated wires

In order to evaluate the influence of lamination process on the conductivity of printed wire on PET, the resistance characteristics of functional wires were further analyzed. Since the conductive wires in each pattern (I-X) varies, the relative

changes of resistance were determined to get comparable values. The relative change of resistance (R_i/R_0) for laminated wires were calculated by dividing the measured resistance of laminated conductors (R_i) with reference resistance (R_0) of same patterns of samples B1 and B2. Obtained results are summarized in Fig. 3.

Lamination process was observed to improve the conductivity of printed wires. This phenomenon is also observed in other studies [30-31]. Performed curing is not ideal in R2R process due shorter curing time and lower temperature than the manufacturer recommends. In addition, the pressure during the lamination is also expected to improve the percolation of metal particles, resulting in the improved conductivity of the printed wire. [30-31] The improvements for the conductors without surface mounted connectors (II-IV, VI-IX) was 9 % in average and 18 % respectively for the wires with surface mounted connectors (I, V, X).

In addition, the measurement results show that surface mounted connectors (B1 type) decreases the resistance about 20 % in contrast to the wires without connectors (B2 type).

C. Absolute resistance characteristics of laminated wires

The absolute resistance of printed conductors depends on many variables such as physical dimensions (width, thickness, length), printing and annealing parameters, lamination etc. Two different and representative patterns (V, VI) were analysed. The pattern V represents a sample with surface mounted connectors while pattern VI is pattern without connectors. The higher the wire ID, the shorter the conductor (V.1 is longer than V.2). Obtained results are shown in Fig. 4 and Fig. 5.

Based on theory, the resistance of conductive wire is linearly proportional to the length of it (assuming that cross-section is constant) [32]. This characteristic is greatly supported by the experimental results obtained from both patterns (Fig. 4 and Fig. 5.). However, due to the fact that the physical dimensions of the wires in patterns VI and V are different, their absolute resistance values vary.

Knowing cross-sectional area (*A*) (measured by optical profilometer), length (*L*) and absolute resistance of the
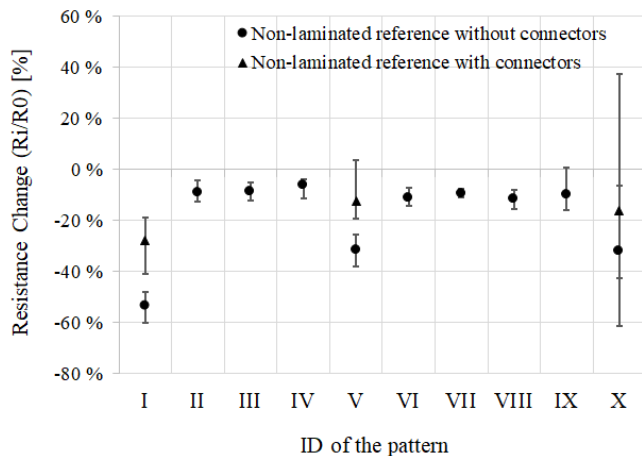
Fig. 3. Relative change of resistance after lamination. Two different type of reference samples were used to distinguish the effect of surface mounted connects.
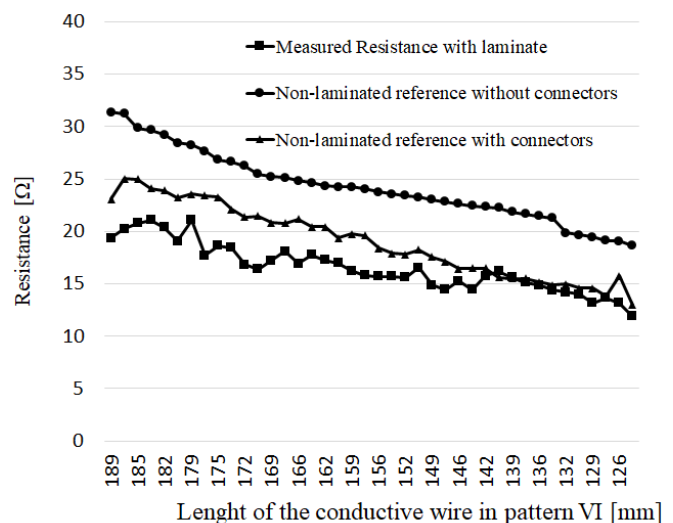
Fig. 4. Resistance of conductive traces in pattern (V.1-V.40). The absolute resistances of the wires are linearly proportional to the length of trace.
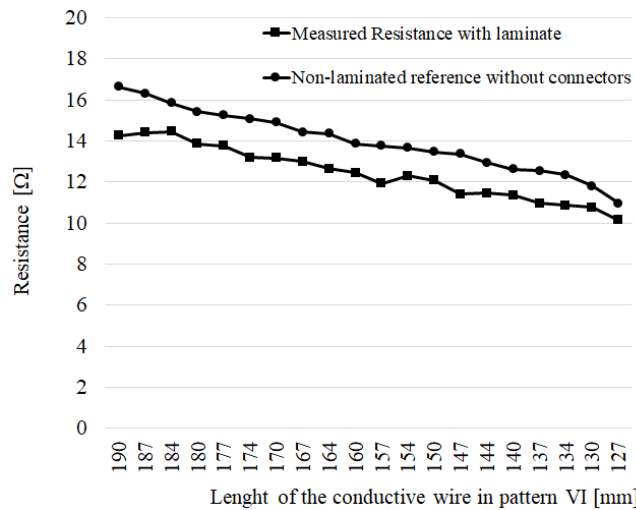
Fig. 5. Resistance of conductive traces in pattern (VI.1-VI.20). The absolute resistances of the wires are linearly proportional to the length of trace.

conductor (R) the electrical resistivity (ρ) can be calculated by the Eq. 1.

$$\rho = \frac{RA}{L} \qquad (1)$$

Cross-sectional area of wires of sample B2 in pattern VI.9 was measured to be 4.5e-3 mm², the length of the corresponding wire was 163.6 mm. Thus, the resistivity of the printed silver wire is 3.9e-7 Ωm. The value agrees with the specified volume resistivity of 4.0e-7 Ωm for Asahi LS-411AW. Since the measured resistance is linearly proportional to the length of wire (Fig. 5.), resistivity is similar in all the printed wires of the pattern. Assuming that lamination does not significantly influence on the physical dimensions of the wires, the resistivity of laminated conductors is 3.5e-7 Ωm.

D. Inspection of structural changes caused by lamination

Resistance measurements are appropriate to characterize production yield of laminated conductors, but they do not
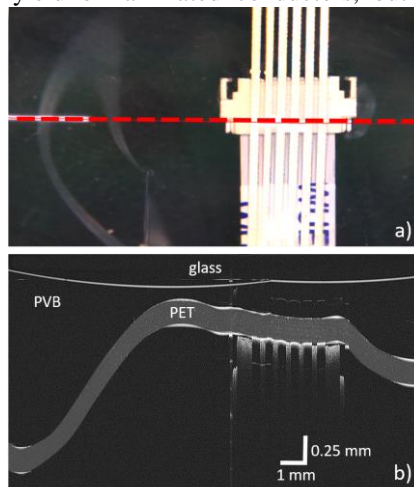

Fig. 6. Image of the connector with the distorted light reflections from PET (a); OCT cross-sectional image along the dashed line with emphasized PET film (b). Images are stitched from two measurements. Due to optical aberrations, the glass-PVB interface appears to be curved. The vertical scale bar is depicts optical distances.
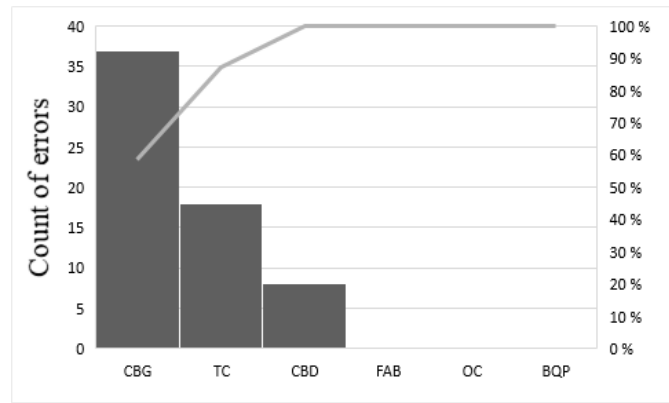

Fig. 7. Results of Pareto analysis for causes that leads to catastrophic failure in the printed conductors and affecting the production yield. Conductor broken due graze (CBG); Tilted connector (TC); Conductor broken due delamination (CBD); Failures at component assembly and bonding (FAB); Oxidation of conductor (OC); Bad printing quality (BPQ)

provide much information about the causes for the observed results. Thus, additional structural analysis of the laminates was done using visual inspection and OCT analysis. The observed key findings are briefly summarized in this section.

All the laminates look visually good and there is not any cracks on glass. Some excess PVB on the edge of laminate were observed. Due to the fact that part of the PET is outside the glass laminate, printed silver traces are oxidised (slightly brownish color) and partially detached from PET during the lamination. Visual inspection also reveals that some of the surface mounted connectors are dislocated during the lamination thus having impact on yield of those patterns (I, V and X).

Further OCT characterization were done in the regions on the proximity of surface mounted connectors. As shown in Fig. 6, the PET film is bended explaining the distorted light reflections from these areas. This is naturally modified by the thermomechanical stress distribution caused by lamination, and thus probably influencing on the yield of those patterns. However, further analysis and thermomechanical stress simulations are needed to confirm this observation.

E. Pareto analysis

Results of Pareto analysis are shown in Fig. 7. The results are based on the failures of each pattern per laminate. Only exception is the failure mechanism, which involves a connector. In case failure involves a connector, the results are based on patterns I, V and X. According to the analysis, most of the catastrophic failures in the samples can be explained by a broken conductor due graze (CBG) which occurred unsystematically in different patterns and had a count of error (COE) of 37. The second most impactful cause for failures was a tilted connector (TC). Tilting was most common at the both edges of the laminate. COE for the tilted conductor was 18. The third most impactful cause for failures, of which COE was 8, was a broken conductor due to delamination (CBD). Delamination also occurred unsystematically in different laminates as well as the grazes on conductor. Other causes for failures such as oxidation of conductor (OC), failures at component assembly and bonding (FAB) and bad printing quality (BPQ) had COE count of 0.

IV. DISCUSSIONS

The production yield of each patterns varies depending on their properties (see Fig. 2). Printing and assembling the component can also act as a source for variations of production yield. In this study, conductors and component assembly were tested before the lamination hence the effect of production to TPY can be excluded.

The patterns with the surface mounted connectors have lower yield, which is problematic because they are favorable for many applications due to the better electrical conductivity. In addition, surface mounted connectors have standardized interfaces making them more compatible with other electronics. The reason for lowered yield can be partially explained by the high number of wires, smaller width of them and therefore lower tolerance for inaccuracies. Tension and consequent bending of PET due to stress at surface mounted connector during the lamination process may also affect to electrical functionality and lower the yield. Although this kind of tension affects on the yield, it does not completely explain the catastrophic failures in conductors and, according to earlier articles, it is possible to reduce the impact of this type of tension to conductor's condition by growing the thickness of the conductor, which on the other hand decreases its durability to cycling bending [33-34]. Another solution for lowering the tension could be to modify the process parameters by lowering temperature and thus lowering thermal stress [35]. In addition, the patterns I and X were at the proximity of the corner of the laminate where the thermomechanical stress in lateral direction is expected to be the highest during the lamination thus having increased risk for dislocated connectors. However, the reasons for the decreased yield of the conductor patterns with the surface mounted connectors requires further investigation.

In all of the cases, the average conductivity of patterns (I-X) was observed to be increased by the lamination. It is worth to mention, that in the case of surface mounted connectors, conductivity improvement of the patterns was even more than without them. That can be explained by the fact that the conductors of the connectors have much higher conductivity than printed wires. Once the connectors are mounted on the surface, part of the printed conductors are bypassed with better conductive wires, reducing the absolute value for measured resistance.

According to the Pareto analysis the most impactful cause for critical failures in the samples was the grazes on the conductors outside of glass lamination that were most likely independent of the process. The grazes were most likely caused by a sharp object or sharp edge, which should not be the case in the lamination process. Hence, grazes are most likely occurred during transportation, preservation or measurements. Therefore, even if the lamination causes thermomechanical stress and creates challenges especially when using SMD components, the process itself may not be that harmful to conductors and may even be rather beneficial due the improved thermal and electrical conductivity. Still, using SMD components inside glass laminate requires additional designing due to thermomechanical stresses, which are expected to be the highest at the corner of the glass laminate and causing dislocated components.

From laminated electronics commercialization point of view the lifetime of the products is important. Lamination process itself is expected to have a significant impact on electronics lifetime. However, this study does not reveal the aspects of long-term reliability of laminated electronics and thus further research is needed.

V. CONCLUSION

According to this study, printed electronics lamination inside the glass is possible. Knowledge gained about the failure mechanisms from the Pareto analysis can be utilized to improve electronics design, material selection and process optimization in order to obtain a high electrical functionality and production yield. Lamination was also observed to improve the electrical conductivity of printed conductors. In order to make justified design rules and manufacturing guidelines for these type of products further studies are required. However, gained expertise is expected to accelerate the commercialization of glass laminated electronics for example in automotive industry and as architectural elements.

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