A 28 GHz Static CML Frequency Divider with Back-Gate Tuning on 22-nm CMOS FD-SOI Technology

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***Abstract* — A divide-by-2 frequency divider circuit was designed using 22-nm CMOS FD-SOI technology. The circuit utilizes back-gate biasing which provides almost 4GHz additional output center frequency tuning range over other mechanisms leading to 21.3 to 30GHz operation range with 0dBm input signal. This covers 5G bands from 24.25 to 27.5GHz with good margin. Divider dissipates 11mW from 0.86V supply and occupies 800µm^2 of area. Small area allows to place divider-by-2 block next to IQ mixers in a direct conversion or sliding IF transmitter or receiver.**

***Index Terms* — mmWave, divider, CMOS SOI, 5G**

I. Introduction

Emergence of 5G communication standard development has sparked a large amount of research effort into millimeter wave (mmWave) circuits and systems. For years, cost-efficient and high integration capability CMOS processes have been utilizing resonator structures to provide sufficient performance at mmWave frequencies. These structures are bulky. Especially if every radio frequency circuit block needs an inductor, overall area grows excessively large in multi-channel MIMO transceivers. Recent advances in semiconductor manufacturing technologies have boosted CMOS transistor speeds to a level that allows inductorless mmWave circuits, generally at some cost of power dissipation. In frequency generation that uses phase locked loops (PLL), the voltage controller oscillator (VCO) occupies at least one inductor. So the design of the PLL becomes challenging if other PLL blocks also need many inductors. Frequency division at mmWave frequencies is classically done with injection locking frequency dividers (ILFD), which require some resonator structure [1]. ILFD are narrowband but operate with low power. Inductorless alternative to ILFDs is current mode logic dividers (CML), which are split into two categories: dynamic and static. Dynamic dividers are low power and narrowband while static can be made more broadband at the cost of power and small speed penalty [2]. Advantage of static frequency dividers is that some variants can provide differential I/Q phases, which can be used in (de)modulation, for example [3]. Especially in mmWave circuits, broadband I/Q phase generation is valuable feature because passive alternatives such as poly-phase filters are very lossy and require power hungry buffers in the inputs and outputs [4].

In this paper, a static CML frequency divider is proposed. Design is implemented with a 22-nm CMOS FD-SOI process, which is paving the way for high performance mmWave CMOS phased array systems amongst others.

II. Circuit Design

Frequency divider schematic is presented on Fig 1. It consists of two cascaded and fed-back flip-flops. Flip-flop has 4 parts: input differential pair, latch, input clock transistors and a resistive load. The input signal is fed to the clock transistors, which steers the current between differential pair and latch. Differential pair transistors act as flip-flop data inputs and latch transistors to save the input state when clock signal is low. When cascaded and fed-back, the flip-flops divide the input frequency by two.

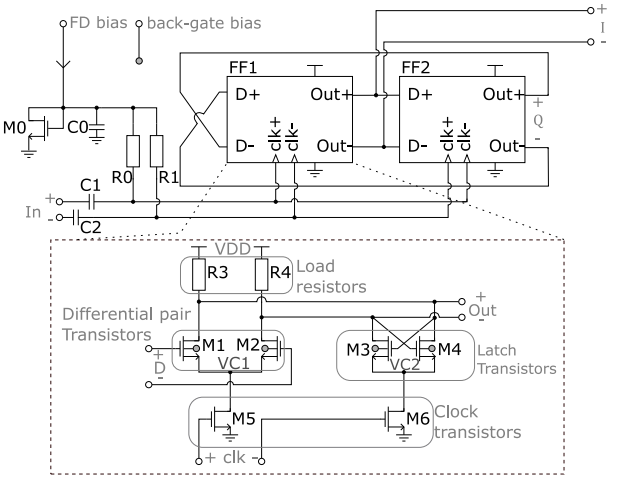

Fig. 1. CML frequency divider schematic. Input balun and output driver are excluded.

The circuit is designed to have minimum time constant in the output nodes and to have enough gain to ensure self-oscillation, which occurs when gain composed by the load impedance and differential pair transistors is higher than unity. In addition, clock transistors are designed to have sufficient drain to source voltage to operate them in active

region thus allowing good coupling of input signal to the flip-flops. Load resistors R3 and R4 are sized to 145Ω. Differential pair and latch transistors are 10.5µm wide and have back-bias connection to an off-chip voltage source. Back-gate bias or back-bias is a connection to transistor well below insulating buried oxide layer and allows tuning of transistor threshold voltage [5]. Back-bias helps tuning the operation point of the divider and to compensate process variation. Additionally, it enables center frequency (f_{so}) tuning by adjusting speed of differential pair and latch transistors. Clock transistors are 15.5µm and are nominally biased to carry 2mA of bias current and have back-bias connection to supply voltage to maximize their current per width to reduce area and load to the preceding stage. In this case, the inputs are driven with a resistive load active balun, which converts single ended signal to differential. Finally, one differential output is buffered with a three-stage common source driver to reduce loading of the frequency divider and to drive the output to 50Ω load. All transistors in the design use minimum gate length of 20nm and 500nm finger length. Layout was optimized by minimizing output node capacitances for maximum speed. Also, series resistances on current paths required careful routing strategy with higher metal layers for low resistance. Divider speed is not sensitive to VC1 and VC2 node capacitances. Hence, clock transistors were placed in a way that keeps minimum distances between the two flip-flops outputs.

III. Measurements

Frequency dividers are commonly characterized using input power sensitivity curve which represents how much input power is required to operate the frequency divider at given frequency. Measurements were performed on-wafer using Cascade Microtech Infinity I67 Probes and Keysight N5242A PNA-X 67GHz vector network analyzer as a signal source and Keysight E4446A 44GHz spectrum analyzer for output measurement. In addition, one Keysight 11612B 50GHz bias-T was used to feed DC-bias to on-chip balun and another in the output to provide wideband DC-blocking to protect spectrum analyzer. Input power was calibrated to probe tip.

Frequency divider micrograph is presented in Fig 2. Divider core takes only 0.0008mm^2 of area, with balun and output driver the area is 0.0031mm^2 and with pads 0.087mm^2.

Measured sensitivity curves are shown in Fig. 3. The frequency divider can be tuned in three ways: supply voltage, input bias and back-gate bias. Increase in supply voltage increases voltage budget on the flip-flops increasing gain and improving coupling of input signal thus increasing bandwidth as well. Input bias adjusts bias currents of flip-flops. This should be sufficiently high to

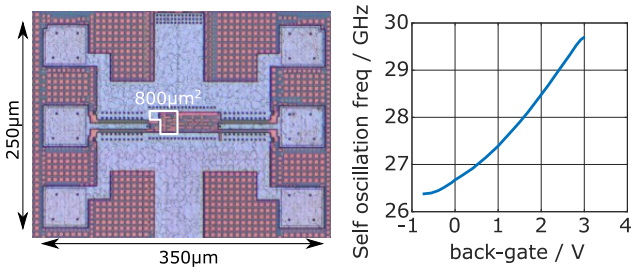

Fig. 2. Frequency divider chip micrograph and back-bias effect on f_{so}. Divider core is highlighted.

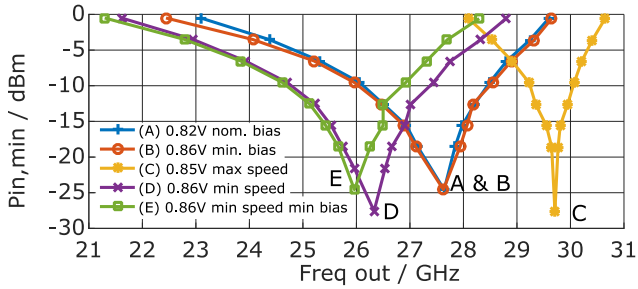

Fig. 3. Measured sensitivity curves.

enable self-oscillation but not too large to prevent clock transistors from operating in triode region. Finally, back-gate bias adjusts the threshold voltages of latch and gain transistors effectively affecting the speed of the divider i.e. center frequency. Higher back-gate bias lowers threshold voltage increasing the center frequency as depicted in Fig 2. First curve (A) shows the sensitivity curve on nominal bias and supply setting. In B curve, the bandwidth is maximized by boosting supply voltage and minimizing bias. C curve shows maximum speed setting when back-gate bias is at maximum and last two curves show behavior with minimum back-gate bias. Overall bandwidth achieved with bias current and back-gate bias adjustments is 21.3 to 30.6GHz resulting to 36% fractional bandwidth. With fixed input bias and back-bias, the fractional bandwidth is 22.4 to 29.6GHz or 28%. Back-bias allows tuning of center from 26.4 to 29.7GHz. Even further tuning range is possible without ESD protection limits, which limit the back-gate bias to above -0.8 and below 3.5V in this chip.

Phase noise of the divider was measured with R&S FSW 50GHz spectrum analyzer. Fig. 4. has phase noise curves of 48GHz reference input signal and of output signals on three bias points B, D and E at 24GHz (from Fig. 3) to see the effect at the edge of the bandwidth on phase noise. If bias current is too low (E setup) the phase noise degrades. Below 4MHz offset, the average phase noise drop for B, D and E is 5.89dB, 5.98dB and 5.06dB respectively, proving the theoretical 6dB phase noise reduction on divide-by-2 operation. Noise of the measurement system flattens the measurement curve above 4MHz.

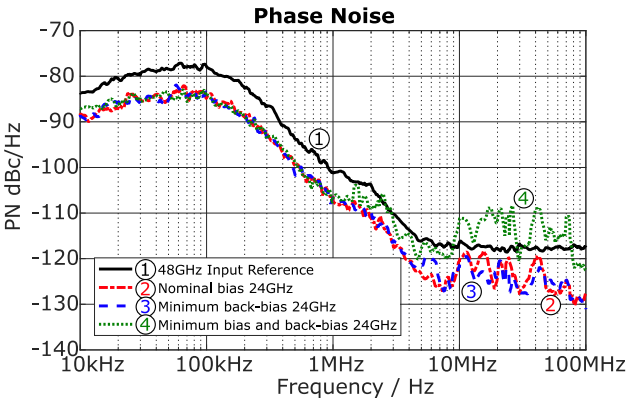

Fig. 4. Measured input reference and output phase noise.

IV. Comparisons

Static inductorless CML frequency dividers for mmWave frequencies made with CMOS are relatively rare compared to dynamic or injection locked dividers. Table I compares wideband dividers over available tuning ranges and taking power dissipation from middle of band configurations. 22nm technology process allows the use of very small supply voltage compared to the other for similar frequency range. One State-of-the-Art ILFD is also compared. It has good Figure-of-Merit from wide bandwidth and low power but at the cost of area.

TABLE I
CMOS Wideband Frequency Divider Comparison

Reference	This work	[7]	[8]	[2]
Process	22nm FDSOI	90nm	65nm SOI	65nm
f_{so} (out) [GHz]	26.4-29.7	24	32.5-42.5	~47
Bandwidth [f_{low}-f_{high}]	21.3-30	2-27	<32-47	32-62
Power [mW]	11	39.7	35.2	1.2
Supply	0.86	1.5	2.4	0.42
Area mm^2	0.0008	0.02	0.0016	0.07
FoM	7.28	8.69	5.24	104.7

$$FoM = \frac{Locking\ Range\ (\%) \cdot Division\ Number}{P_{in}(mW) \cdot P_{DC}(mW)} \quad (1)$$

Figure-of-Merit used in the table takes into account the input power, locking range and power dissipation as defined by (1) [6].

VII. Conclusion

A mmWave static divide-by-2 CML frequency divider was designed and manufactured using 22-nm FDSOI, resulting in small area and wide tuning range with inductorless design at mmWave. Tunability with back-gate bias and FDSOI properties provide valuable leverage against process variations to which this circuit topology is notorious for. Circuit operates from 21.3 to 30.6GHz with 0dBm input signal and has center frequency adjustable from 26GHz to 29.6GHz relaxing preceding stage drive requirements at these frequencies. Frequency range, reasonable power consumption of 11mW and I/Q outputs make this circuit very suitable for 5G applications and other mmWave systems.

Acknowledgement

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