Layout Optimization Techniques for r_g and f_{max} of Cascode Devices for mmWave Applications

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***Abstract* — A common-source cascode device is commonly used in amplifier designs at RF/mmWave frequencies. In addition to intrinsic parasitic components, extrinsic components due to wiring and layout effects, also play an important role towards performance and accurate modelling of the devices. In this work, a comparison of two different layout techniques for cascode devices is presented, to reduce the extrinsic parasitic elements, such as gate resistance. A multi-gate or multi-port layout technique is proposed for optimizing the gate resistance (r_g). Two separate structures are designed and fabricated using 45nm CMOS SOI technology. Extracted values from measurement results show reduction of 10% in r_g of multi-gate layout technique compared to a conventional gate-above-device layout for cascode devices. However, conventional layout exhibits smaller gate to source and gate-to-drain capacitances which leads to better performance in terms of speed, i.e. f_{max}.**

***Keywords* — mm-wave, RF, LNA, receiver, 5G, multi-gate, communication systems, CMOS, SOI.**

I. Introduction

One of the key requirement for next generation communication systems, i.e. 5G, is the bandwidth of a channel from few hundred MHz to 1 GHz. Therefore, mm-wave frequencies are selected for future 5G systems where at least 1 GHz bandwidth, is available at multiple frequency bands, e.g. 24 GHz, 28 GHz and 40 GHz, etc. CMOS technologies are providing scalable and integrated solutions for faster and wideband mm-Wave systems.

CMOS silicon technologies are characterized with its performances in active devices and passive structures. Maximum speed of the active devices is governed mainly by the gate length of a single transistor and its intrinsic components. As the frequency of operation is increased, small intrinsic components, e.g. capacitances, become significant and draw a limit for operation. Maximum frequency of operation of a single transistor is limited due to f_{max} and performance of passive structures depends on the availability of thick metal stack with low metal resistance and resistivity of the substrate. Higher the resistivity, lower are the losses and higher the quality factor (Q) in passive structures. In amplifier designs at mmWave frequencies, design of active devices for optimum performance parameters, i.e. current density (J), transconductance (g_m), input and output capacitance and isolation from output to input to avoid any instability, are very important. High frequency performance (f_{max}) of an active device depends mainly on the intrinsic components such as

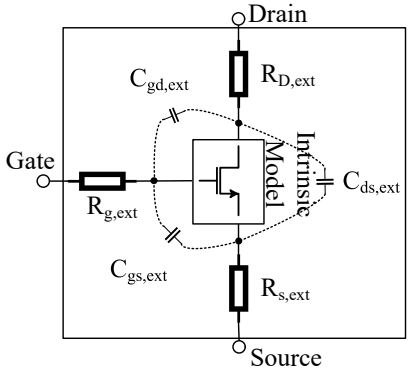

Fig. 1. Extrinsic components of an NMOS transistor

g_m, gate resistance, r_g, and total gate capacitance, c_{gg}. In addition to these intrinsic components, which are included in the model of the device, extrinsic components due to wiring for interconnects are also critical to further limit the f_{max}. In modern CMOS technologies, intrinsic model of a transistor can include wiring parasitic up to higher metals in the metal stack. But still the inductance of the interconnect, i.e. top layer via, are critical for mmWave frequency operations. Fig. 1 shows a picture of main contributors to gate resistance from interconnection to thick metal layers. Extrinsic gate resistance of transistor mainly composed of metal resistance of m1 ring around the transistor fingers and number of vias used to connect the m1 ring to thick metal for signal routing. However, because of rather large dimensions and design rule limitations of thick metal vias, number of such via connections are limited by the dimensions of the transistors.

Cascode devices are used to design amplifiers and variable gain amplifiers, etc. because of its benefits, e.g. improved gain and better isolation between input and output. When laying out the devices in a conventional way, additional parasitic components due to wiring, also appear at the drain and source junction of two transistors. Multi-gate layout technique has been used to eliminate metal contacts in intermediate node of stacked (cascode) transistors to reduce interconnect parasitic components [1] [2]. Additionally, multi-gate technique can also be useful to increase the number of thick metal vias, which can help in reduction of extrinsic gate resistance. However, while

laying out larger devices, wiring multi-gate layout designs also brings additional capacitance from gate to drain terminals of the device which limits the overall f_{max}. Therefore a tradeoff between r_g and f_{max} exists in the layout of cascode devices. In this paper, we design and compare cascode transistor devices using conventional gate-above-device layout technique [3] and multi-gate technique. Two separate layout structures for cascode devices are designed and fabricated in 45nm CMOS silicon on insulator (SOI) technology. The measurement results show an reduction of gate resistance for multi-gate device, with somewhat degraded f_{max} due to increased c_{gg} compared to conventional device.

In this paper, section II describes design of cascode devices and its layout effects. Section III presents experimental results. Conclusion of the paper is given in Section IV.

II. Cascode Devices

In order to create understanding and a reliable model for active devices at mmWave frequencies, interconnects between different structures should also be taken into account. Wiring of active devices upto lower metal layers are included in the intrinsic model of the device. However, intermediate interconnects from lower metal layers to thick metal layers should be extracted carefully using electromagnetic tools, which completes an accurate modelling of the transistor for mmWave frequency designs. Gate resistance of the input transistor affects the speed and noise performance of an amplifier. In addition to intrinsic gate resistance $R_{g,int}$, external wiring and interconnects also contribute to overall R_g of the transistor as given in (1) [4].

$$R_{g,tot} = R_h + R_v + r_{via,int} + r_{via,ext} + r_{wire} \qquad (1)$$

Where R_h and R_v are horizontal and vertical resistance of a single gate finger, respectively. r_{via} is the resistance of poly to metal contact and r_{wire} is the resistance of interconnect for external wiring. R_h and R_v are included in the intrinsic model of the device. While r_{wire} and part of the r_{via} depend on the external routing. All of these contributors can be reduced to an optimum value by using efficient layout techniques. For example, increasing number of fingers and gate contacts for each finger helps to significantly reduce in values of r_h, r_v, and r_{via}. Intrinsic interconnect $r_{via,int}$ is the resistance from poly to m1 and can be reduced by connecting each gate poly at both ends, as shown in Fig. 2. Dual gate connection feature upto higher metal layers, e.g. m1, is available in intrinsic model of modern CMOS technologies. $r_{via,ext}$ is the extrinsic resistance of via from m1 to thick metal layers, e.g. m7. This resistance can be reduced by increasing the number of contacts. However, due to larger dimensions of these vias, minimum distance between other interconnects at source and drain nodes of the device is also required to reduce coupling. Another approach can be utilized to route the gate signal at intermediate and semi-thick layer, e.g. m5, over a vertical orientation transistor and connect it at two ends of the device with m1 ring, as shown in Fig. 2. This m5 line can be connected further to

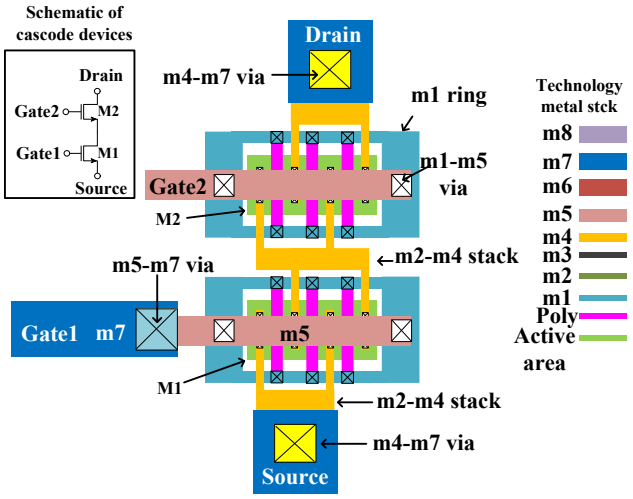

Fig. 2. Conventional-style schematic and layout of cascode devices

thick metal layer at sufficient distance from the device. For example as shown in Fig. 2, only two m1-to-m5 vias can be employed to connect m1 ring of each multi-finger transistor of width 10um. Similarly, source and drain connections are extended further using stack of m1-m4 metal layers, at bottom and top of the devices, where they are connected to m7 layer.

In addition to various benefits, cascode devices have also limitations of the voltage swing for low voltage power supply designs, and additional wiring capacitance at intermediate node and at the output node. In very high mm-Wave frequency designs, inter-stage matching is used to resonate out the wiring capacitance between the transistors [2]. Multigate technique for stacked devices proposed in [1], is helpful in reducing inter-stage wiring parasitics. In this work, we design and compare two layout techniques for cascode devices, i.e. conventional style and multi-gate style, in 45nm CMOS SOI technology. Proposed multi-gate style layout helps not only to reduce inter-stage wiring as discussed in [1], but also allows a larger number of m1-to-m5 vias implemented for the same area of devices compared to conventional layout. This increased number of m1-m5 vias help to further reduce $r_{via,ext}$ in (1).

Transistor layouts for both styles having 20 gate fingers are selected. Fig. 2 shows a conventional gate-above-device layout style of a cascode device [3]. Two transistors are placed in a vertical orientation on top of each other. To reduce $R_{g,int}$ of transistors, gate fingers are connected at both sides using a ring of metal m1. Input signal from a ground-signal-ground (GSG) pad is routed at metal m7 and brought to m5 near the gate of common-source device M1, which is routed over the transistor and connected gate ring at metal m1 from two sides, as shown in Fig. 2. In order to achieve enough current handling capability of metals, source and drain connections of each finger is brought up to metal m2 to m4 and connected together with a wider stack of metal layers from m2-m4. These connections are extended further to each direction and connected to thick metal layer m7. This further extension of drain and source connections helps to reduce the additional

capacitive coupling due to thick metal lines between different nodes, e.g. $c_{gg} = c_{gd} + c_{gs}$.

Multi-gate layout technique is drawn by sharing the active area of two transistors to eliminate intermediate metal contacts of drain and source terminals between the transistors for cascode devices [1][2]. A unit cell of a 1um finger width using multi-gate technique is shown in Fig. 3a. Each cell has double connected gate finger at metal m1. Source and drain connections are extended further from the device using stack of metal m2-m4. A distribution network of such cells is placed in a vertical orientation such that the gate connection at metal m1 is shared between two cells. An m1-m5 via is placed in this shared area of gate at m1. This increases the number of vias at gate terminal. Gate signal is routed at metal m5 from top of the structure and tapped to the gate contacts using these m1-m5 vias. A device schematic and layout schemes are shown in Fig. 3b, which is composed of 20 unit cells in a tree configuration. Similarly, source connection of the cells are shared between two cells and routed from the middle of the unit cells towards bottom of the structure not crossing the gate wiring to minimize the gate to source capacitance. Similarly, drains of the cells are connected to metal m7 and routed from two sides of the structures to bottom of the structure. As it can be seen from Fig. 3b, there are atleast four times the number of m1-to-m5 vias than used in structure in Fig. 2 to reduce $r_{via,ext}$. Similarly wiring resistance is halved by routing the gate signal at metal m5 in two parallel branches, which helps to reduce the r_{wire}. The layout presented in Fig. 3b is good for optimizing $r_{g,ext}$. However, due to the increased wiring at the drain terminals of the structure, c_{gd} is increased, which limits the f_{max} of the device.

III. Measurement Results

To validate the idea of the reduced gate resistance of a common-source cascode devices using multi-gate technique, two separate structures are fabricated using 45nm CMOS SOI technology. The first is using conventional gate contact, and the second utilizes multi-gate technique. Schematic of the measurement configuration and die micrograph are shown in Fig. 4. S-parameter measurements are performed from 30 to 50 GHz frequency range, using Keysight 67 GHz PNA. GSG pads and probes are used to measure the s-parameters at the input and output. Two port calibration is performed up to the probe tip using external through-reflect-load (TRL) structures on a separate calibration substrate. DC biasing for common source gate and drain of the structures are provided using bias-T from external sources (VDD=1V). Gate resistance of the structures are extracted from the measured s-parameters (at fixed bias voltage of 580mV) and plotted in Fig. 5. Method of extraction for R_g is given in [4]. Measurement results include the input and output pads and extended transmission lines up to the devices. Extracted gate resistance of the multi-gate layout technique is 10% lower than the conventional layout style. Due to the increased wiring of the multi-gate technique, gate to source (C_{gs}) and gate-to-drain capacitance (C_{gd}) are 4% and 40% higher than the conventional layout, as shown in

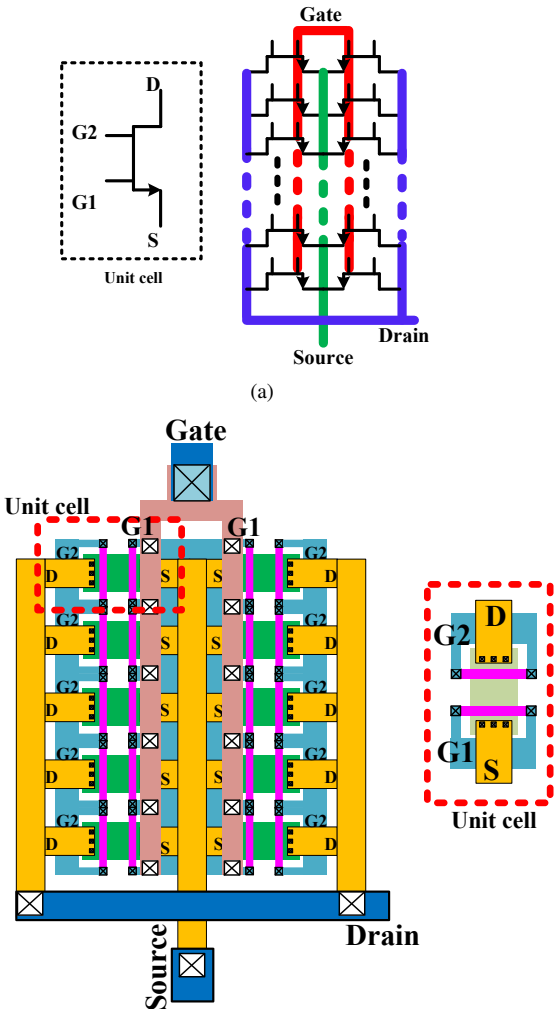

Fig. 3. Multi-gate device schematic and layout (a) Single unit cell and multi-cell schematic (b) Layout of single cell and multiple cells

Table 1. Comparison Table of Extracted Parameter Values at 40 GHz (VDD=1V, V_{bias}=580mV)

Parameters	Conventional	Multigate
R_g (Ohms)	14.3	12.9
C_{gs} (fF)	60	62
C_{gd} (fF)	2.77	4.33
g_m (mS)	22.5	22.5
f_{max} (GHz)	243	215

Fig. 6. There is no change in the transconductance (g_m) of both structures, as shown in Fig. 7. For C_{gs} , C_{gd} and g_m extraction, methods given in [5] are used. Due to the increase in C_{gg}, f_{max} of multi-gate device is 20% lower than the conventional layout as shown in Fig. 8. However, this is still sufficient for targeted frequency bands. Since the available modelling for multigate devices differs from the conventional transistors, therefore, simulations are not shown for comparison between two structures. Table 1 shows comparison results of extracted parameters at 40 GHz for the two structures.

IV. Conclusion

This work introduces layout optimization techniques of cascode connected transistors for mmWave applications. A

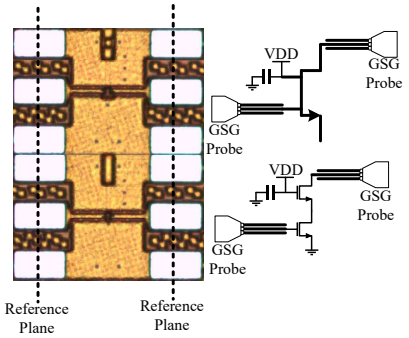

Fig. 4. Die micrograph of cascode structures and respective schematics.

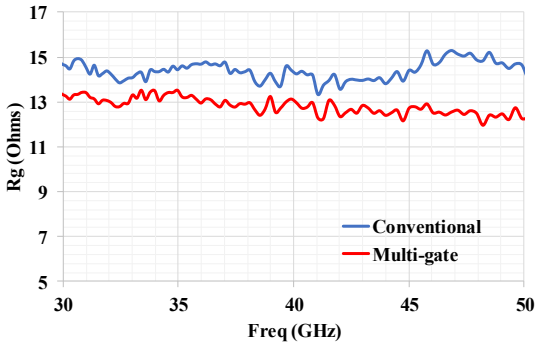

Fig. 5. Extracted R_g of two structures, (VDD=1V, V_{bias}=580mV)

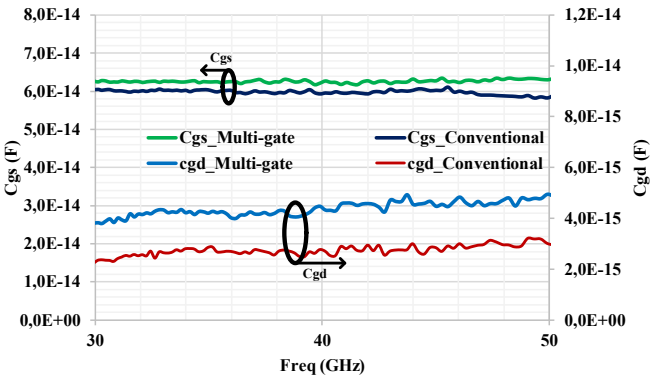

Fig. 6. Extracted capacitances, C_{gs} and C_{gd} of two structures, (VDD=1V, V_{bias}=580mV)

multi-gate layout technique is compared to a conventional layout style. Optimization of intrinsic and extrinsic parasitic components for both cascode devices is discussed. A multi-gate layout reduces gate resistance while conventional layout reduces wiring capacitance. The compared cascode devices are designed and fabricated using 45nm CMOS SOI technology. Measurement results at mmWave frequencies, show an reduction of 10% in gate resistance of multi-gate layout technique compared to the conventional double contacted gate approach. However, gate-to-source and gate-to-drain capacitances are degraded by 4% and 36%,

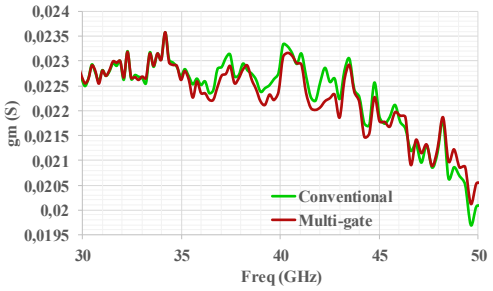

Fig. 7. Extracted g_m of two structures, (VDD=1V, V_{bias}=580mV)

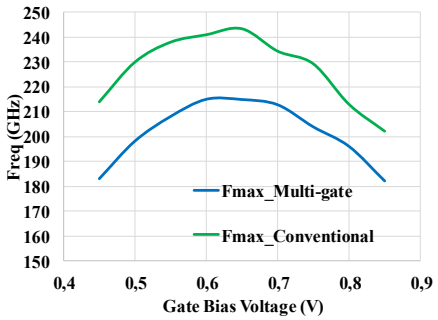

Fig. 8. Extracted f_{max} vs V_{bias} of two structures

respectively, which limits the maximum speed of devices. Therefore, this comparison concludes that there is a trade-off in optimizing between r_g and f_{max} of the cascode devices in layout designs.

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