A 3.5-GHz Digitally-Controlled Open-Loop Fractional-N Frequency Divider in 28-nm CMOS

Tze Hin Cheung*, Mikko Martelius*, Yury Antonov*, Rehman Akbar†,
Jussi Ryyänen*, Aarno Pärssinen†, Kari Stadius*

*Dept. of Electronics and Nanoengineering, Aalto University, Finland

†Centre of Wireless Communications – Radio Technologies, Oulu University, Finland

Abstract—This paper describes the design and measurement of an open-loop fractional frequency divider implementation. The fractional divider consists of a multi-modulus integer frequency divider (MMD), a sigma-delta modulator (SDM) and a pipelined phase interpolator. The fractional frequency division is achieved with the MMD and the 13-bit SDM toggling the integer division ratio. The resulting signal is then processed by the phase interpolator which significantly reduces the spurs by 22 dB and generates spectrally clean signal with correct output frequency. The prototype is implemented in 28-nm CMOS technology and it operates within input frequency range of 1.9 GHz – 3.5 GHz with fractional division ratio in between 2–3. As an example of the operation, with a setting of an arbitrary division ratio of 2.3164 and input frequency of 2.4 GHz, the output sets correctly to 1.0361 GHz with RMS jitter of 2.1 ps.

I. INTRODUCTION

Present-day system-on-chip (SoC) communication circuits include sets of LO and CLK domains for wireless and digital signal processing. While fractional-N phase-locked loops [1]–[3] provide the main LO signals with highest purity, agile frequency planning for clock generation and moderate performance LO signals calls for other solutions as well. Direct fractional frequency division is one attractive candidate for enabling flexible and multi-purpose clock and LO signal generation for future SoCs. The purpose of such a divider is to further increase the range of synthesizable frequencies and improve resolution while maintaining low spur level.

In this paper, we present the design and measurements of an open-loop fractional frequency divider which consists of a multi-modulus integer frequency divider and a first-order 13-bit $\Sigma\Delta$ -modulator. The modulator controls the operation of the integer divider in such a manner that the overall division ratio is a fractional value between 2–3. Additionally, we propose a time-based pipelined 8-bit phase interpolator for averaging the duty-cycle of the output signal which in turn reduces the spurious content of the output. In the prototype implemented in 28-nm CMOS technology we have achieved an input frequency range of 1.9–3.5 GHz and a corresponding output frequency range of 0.63–1.75 GHz.

The paper is organized in the following way: Section II covers the fundamental fractional division concept employing the switching of integer division ratios for achieving a fractional value. Section III introduces our proposed open-loop fractional frequency divider. Section IV describes the implementation

Fig. 1. Block diagram of the proposed fractional frequency divider.

and measurements of the proposed design and finally Section V concludes the paper.

II. FRACTIONAL DIVISION CONCEPT

A fractional division ratio can be achieved with a frequency divider with controllable division ratios consisting of at least two different integer values. The fractional division ratio achieved with the toggling operation can be evaluated as

$$\begin{aligned}
 N_{frac} &= \frac{X}{X+Y} \cdot N + \frac{Y}{X+Y} \cdot (N+S) \\
 &= N + \frac{Y}{X+Y} S,
 \end{aligned} \tag{1}$$

where N_{frac} is the fractional division ratio, N is an integer division ratio, X and Y are the enable ratios of the smaller and larger integer division ratios respectively, S is the step size between the integer ratios which is typically one. Fractional division ratios that are depicted using (1), are fractional values achieved by averaging two integers. In other words, the fractional division ratio achieved with this toggling method shifts the fractional resolution from the divider circuit itself into the circuit corresponding to the control of the division ratio of the multi-modulus divider. Precise generation of the control signal is crucial for defining the achievable fractional resolution and the divider also has to be capable of switching the division ratio fast enough in order not to cause glitches to the output signal.

The toggling of the division ratio is produced by a digital $\Sigma\Delta$ -modulator. The modulator is implemented as an accumulator which counts the number of pulses of the divider and

then generates the control signal for toggling the division ratio corresponding to the desired fractional division ratio. This method generates a signal that has the desired fractional frequency as a time-average signal due to the approximation of a fractional value using integer values.

Averaging a fractional value using integers will generate truncation errors in the form of phase offsets. These phase offsets need to be compensated in order to have a clean signal and to minimize the spurious content. Deterministic phase offsets can be reduced with time- or frequency-domain techniques depending on the nature of the feedback used. Closed-loop systems such as fractional-N phase-locked loops use both time- and frequency-domain techniques [1]–[5], whereas open-loop divider designs can only use time-domain methods for the reduction of fractional spurs [6], [7] such as the pipelined phase interpolator in our design.

The phase offsets generated by $\Sigma\Delta$ -modulator depend on the order of the modulator. For a first-order modulator, the phase offsets are one reference period at maximum [8], [9]. Furthermore, a first-order modulator produces phase offsets that are directly related to the amount of residue that the modulator has accumulated. The residue can be calculated in respect to the reference clock that is fed to the divider and thus the residue in itself contains sufficient information to be used as a control word for a phase offset compensating circuit. In contrast, a higher-order modulator introduces additional complexity for the compensation circuit without providing major improvement in the phase noise performance in open-loop fractional frequency dividers [9]. Therefore, first-order $\Sigma\Delta$ -modulator is optimum for our purpose.

III. PROPOSED OPEN-LOOP FRACTIONAL-N FREQUENCY DIVIDER

A. Architecture

In our open-loop fractional frequency divider (FDIV) design, the operation principle described in Section II is implemented with three distinct circuit blocks as is shown in Fig. 1. The proposed FDIV consists of a multi-modulus frequency divider (MMD), a first-order 13-bit digital $\Sigma\Delta$ -modulator (SDM) and an 8-bit pipelined phase interpolator (PI).

In brief, the generation of a fractional division can be divided into three separate tasks which include division, control and phase offset compensation. The MMD divides the input frequency according to the fractional division ratio defined and controlled by the SDM. The resulting signal from this process is then compensated using a pipelined PI. The PI is controlled by the accumulated residue in the SDM, resulting from the fractional division process.

Fig. 2 illustrates the fractional frequency signals after the MMD and PI. The *Output* signal shown in the bottom of Fig. 2 illustrates a compensated fractional frequency signal. In the illustrated signal, the inherent delay caused by the PI is removed for clarity.

The MMD and PI are implemented using differential circuits, but in the upcoming figures the designs are shown using single-ended versions for clarity.

Fig. 2. The relationship of signals within the fractional frequency divider.

Fig. 3. Single-ended block diagram of the multi-modulus integer frequency divider.

B. Multi-modulus Integer Frequency Divider

The core functionality of the FDIV is achieved with a synchronous multi-modulus integer frequency divider. The proposed MMD is designed with differential current-mode logic (CML) latches in a division by 2 or 3 arrangement. The single-ended block diagram of the MMD is shown in Fig. 3. In our design, the division by 2 or 3 is achieved with two flip-flops, two AND gates and a XNOR gate.

The fractional division ratio is achieved by toggling the division ratio. The toggling operation is performed by a digital part that is triggered by the rising edge of the $clk_{\Sigma\Delta}$ signal. The $clk_{\Sigma\Delta}$ is one input period, T_{in} , delayed version of the MMD_{out} . This specific arrangement is used to avoid glitching the output signal during the switching between integer division ratios.

C. Sigma-Delta Modulator

In the developed FDIV, the fractional division ratio is achieved with a first-order $\Sigma\Delta$ -modulator controlling the division ratio of the MMD. The SDM also produces the proper control word for the phase interpolator to compensate the fractional spurs.

The control word to the PI is the residue accumulated in the SDM and as such, no complicated control word transformation is required. This is possible because of specific architecture of the PI complementing the first order SDM. The phase offsets are derived in relation to the T_{in} as the flip-flops forming

the MMD are synchronized to integer time-periods of the reference signal. As an example for a fractional division ratio of 0.4, the accumulated residue follows a pattern: 0.4, 0.8, 0.2 (+ overflow), 0.6, 0 (+overflow) and then the pattern repeats itself. The overflow indicates a change into a higher division ratio. The waveform generated by the pattern is illustrated in Fig. 2.

The delayed output signal of the MMD is the clock signal for the SDM as shown in Fig. 2. The use of a rising edge as a trigger ensures that the division ratio of the MMD does not introduce any undesired glitching of the output when switching the division ratio between two and three.

D. Pipelined Phase Interpolator

In the implemented FDIV design, a phase interpolator is used to perform the phase offset compensation. With the use of a pipelined structure for the PI, each stage of the PI consists of the same interpolating and phase selecting part. The operation principle of the pipelined PI is based on the iterative production of an interpolated phase from two phase offsetted signals in each stage of the PI [4]. After interpolation a pair of signals is selected for the next PI stage for the same process again.

The interpolation process generates a signal with relative phase offset of half the phase offset between the two original signals. For this reason the initial phase offset that is fed to the PI input determines the dynamic range requirement of the PI output. The first stage of the PI consists of a 3-phase generator which generates additional signals with a $0.5T_{in}$ and $1T_{in}$ phase offsets in relation to the MMD output. This initial generation of $1T_{in}$ range input also corresponds to the output range of the PI. This range covers the maximum phase offset producible by the first-order $\Sigma\Delta$ -modulator.

A PI stage consist of three separate PI units and phase selection multiplexers as shown in Fig. 4. Two of the three PI units serve as delay elements for the original two signals that are to be interpolated and the remaining one generates the interpolated signal. A PI unit then consists of a phase interpolating circuit, a Schmitt trigger and capacitor bank as shown in Fig. 4. The interpolation is implemented by using the information provided by a change in the rate of charging and discharging the capacitor banks. The rate of charging and discharging doubles when both of the inputs of the PI Unit are at the same logic level. This information can be used to gauge the time when both of the signals have arrived at the PI units. The waveforms within the three separate PI units are illustrated in Fig. 5. In order to have proper interpolation result, two separate trigger levels for the interpolated signal have to be used: one for the rising and another for the falling edge. These trigger levels are implemented by using a Schmitt trigger which also restores the signal shape. After the generation of the phase interpolated signal, a pair of the signals is forwarded to the successive PI stage. The signal pair consists of one of the two delayed original signals and the interpolated signal. The selection is performed using two multiplexers with the interpolated signal being common to the multiplexers.

Fig. 4. Phase interpolator stage consisting of three phase interpolator units and two multiplexers for phase selection.

Fig. 5. Illustration of the signals within three separate PI units with differing input combinations. A_d and B_d only experience delay, whereas AB is the interpolated signal.

Fig. 6. Chip photo of the implemented fractional frequency divider occupying an area of $630\mu\text{m} \times 270\mu\text{m}$.

In summary, each additional interpolation stage reduces the phase offsets between forwarded signals to half. The optimization of the PI design is thus a design choice between achievable spectral purity of the final output, and area and power consumption. In our prototype, the PI has eight stages.

IV. MEASUREMENTS

The proposed open-loop fractional frequency divider is implemented in 28-nm CMOS technology employing mixed-mode design. The layout of the design occupies an area of $630\mu\text{m} \times 270\mu\text{m}$ and is depicted in Fig. 6.

The circuit is capable of operating between input frequencies of 1.9–3.5 GHz which correspondingly generate output frequencies between 0.63–1.75 GHz while using fractional division ratios between 2–3.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER OPEN-LOOP FRACTIONAL FREQUENCY SYNTHESIZERS

Architecture	This Work Frac-N Divider (MMD + PI)	[6] Frac-N MDLL (Open-loop)	[7] Frac-N Divider (MMD + Delay line)	[10]* Frac-N Divider (MMD + DTC)
Technology (nm)	28	65	65	65
Supply (V)	0.9	N/A	0.9	0.9
Fract. Bits	8	N/A	14	10
Input Freq. (GHz)	1.9–3.5	0.264	5.0	5.325
Output Freq. (GHz)	0.63–1.75	0.4–2.1	0.02–1.0	0.000001–1
Integrated Jitter (ps _{rms})	2.12 (1k–10M)	0.45 (2079 MHz)	1.44 (10k–40M)	1.2
Power Consumption (mW)	86.3 @ 1.0361 GHz	DLL=5 single DPS=12.8 @ 2.1 GHz	3.2 @ 1 GHz	1.17 @ 1 GHz

* Performance parameters from [10] are simulation-based.

The performance of the FDIV is evaluated by RMS jitter and spectrum measurements with different input frequency and division ratio combinations with and without using the PI. The RMS jitter measurements show that the integrated jitter is slightly affected by using the PI, when using the same combination of input frequency and division ratio for the measurement. As an example case of fractional division, the RMS jitter is measured with an input signal of 2.4 GHz divided by 2.3164. This results in an output signal with a frequency of 1.0361 GHz. In this example case, the measured RMS jitter with the PI is 2.12 ps and 3.83 ps without the PI when using 1 kHz–10 MHz band. The measurement with the PI is shown in Fig. 7.

As the integrated noise and RMS jitter measurements are not significantly affected by the use of the PI due to the 1 kHz–10 MHz band in the measurements, the overall performance of the FDIV with the PI can be better evaluated by analyzing a wider spectrum. In Fig. 8, the spectra for the aforementioned example case with and without the use of a PI is shown within a ± 250 MHz band around the output frequency. By comparing the spectra, a clear reduction of spur levels can be noticed when the PI is used. The worst spur within the spectrum is reduced from -15 dBc down to -37 dBc with the use of PI. The integrated power of the spurious content is reduced by 18 dB in the ± 250 MHz band as is shown in Fig. 8.

V. CONCLUSION

In this paper we have presented an open-loop fractional frequency divider consisting of a multi-modulus integer frequency divider, a $\Sigma\Delta$ -modulator and a pipelined time-based phase interpolator. The fractional divider operates with input frequencies within 1.9 – 3.5 GHz while providing fractional division ratios between 2-3 with a resolution defined by the 13-bit $\Sigma\Delta$ -modulator. The pipelined eight-stage phase interpolator cleans the output signal and reduces the worst spurious tone by 22 dB. The prototype demonstrates that open-loop fractional dividers can be used in modern SoC implementations to ease the LO and clock signal synthesis. Future work in this context focuses on simplifying the PI stage structure for better power and area efficiency.

Fig. 7. Measured RMS jitter and phase noise of the proposed fractional divider at an input frequency of 2.4 GHz and a division ratio of $N_{frac}=2.3164$.

Fig. 8. Normalized measured spectrum of the single ended output of the fractional frequency divider with and without the use of phase interpolator. Input frequency is 2.4 GHz and the $N_{frac}=2.3164$. Measured with 500 points.

ACKNOWLEDGMENT

This research has been financially supported by Academy of Finland (grant 2430226211).

REFERENCES

- [1] M. Zanusso, S. Levantino, C. Samori, and A. L. Lacaita, "A wideband 3.6 GHz digital $\Delta\Sigma$ fractional-N PLL with phase interpolation divider and digital spur cancellation," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 3, pp. 627–638, March 2011.
- [2] J. Lin, H. Jiang, and B. Chi, "A 5-bit phase-interpolator-based fractional-N frequency divider for digital phase-locked loops," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017, pp. 1–4.
- [3] R. Nonis, W. Grollitsch, T. Santa, D. Cherniak, and N. Da Dalt, "digPLL-Lite: A low-complexity, low-jitter fractional-N digital PLL architecture," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3134–3145, Dec 2013.
- [4] A. Tharayil Narayanan, M. Katsuragi, K. Kimura, S. Kondo, K. K. Tokgoz, K. Nakata, W. Deng, K. Okada, and A. Matsuzawa, "A fractional-N sub-sampling PLL using a pipelined phase-interpolator with an FoM of -250 dB," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 7, pp. 1630–1640, July 2016.
- [5] R. K. Nandwana, T. Anand, S. Saxena, S. Kim, M. Talegaonkar, A. Elkholy, W. Choi, A. Elshazly, and P. K. Hanumolu, "A calibration-free fractional-n ring pll using hybrid phase/current-mode phase interpolation method," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 882–895, April 2015.
- [6] T. Rapinoja, Y. Antonov, K. Stadius, and J. Rynänen, "Fractional-N open-loop digital frequency synthesizer with a post-modulator for jitter reduction," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2016, pp. 130–133.
- [7] A. Elkholy, S. Saxena, G. Shu, A. Elshazly, and P. K. Hanumolu, "Low-jitter multi-output all-digital clock generator using DTC-based open loop fractional dividers," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 6, pp. 1806–1817, June 2018.
- [8] A. Elkholy, T. Anand, W. S. Choi, A. Elshazly, and P. K. Hanumolu, "A 3.7 mW low-noise wide-bandwidth 4.5 ghz digital fractional-N PLL using time amplifier-based TDC," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 867–881, April 2015.
- [9] S. Tulisi and M. P. Kennedy, "Performance limits for open-loop fractional dividers," in *2017 28th Irish Signals and Systems Conference (ISSC)*, June 2017, pp. 1–4.
- [10] M. Swilam, M. El-Nozahi, and E. Hegazi, "Open-loop fractional division using a voltage-comparator-based digital-to-time converter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 1, pp. 114–118, Jan 2016.