A 290 GHz Low Noise Amplifier Operating above $f_{max}/2$ in 130 nm SiGe Technology for Sub-THz/THz Receivers

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***Abstract*— This paper presents the design of a low noise amplifier (LNA) operating at center frequency 290 GHz in 130 nm SiGe BiCMOS technology with f_t/f_{max} of 300 GHz/450 GHz. The LNA consists of four stages of pseudo-differential cascode topology. Each stage is tuned and matched at different resonant frequency to obtain broadband frequency response around center frequency. This LNA provides 12.9 dB of gain at center frequency 290 GHz and 11.2 dB at 300 GHz. The 3-dB bandwidth is measured to be 23 GHz and simulated noise figure is 16 dB. The LNA draws 68 mA current from 2V supply. It shows the potential of silicon technologies to operate as high as $2/3(f_{max})$ with decent gain and linearity at 300 GHz range. To the authors' knowledge, this LNA achieves, without any gain-boosting technique, the highest gain at $2/3(f_{max})$ in SiGe technology.**

***Keywords*— Low-noise amplifiers (LNAs), sub-millimeter wave and THz Integrated circuits, Receivers, SiGe BiCMOS integrated circuits, VBIC, HICUM, Maximum frequency of oscillation (f_{max}).**

I. Introduction

Due to availability of wide bandwidth, sub-THz and THz frequency bands offer many promising opportunities for future high speed communication such as beyond 5G (B5G) and 6G [1], [2]. It has been analyzed that indoor range for radio link can be achieved at 300 GHz with decent antenna gain and quite moderate noise figure [3]. However, for extremely high data rates of 100 Gbps or above signal bandwidth must be in tens of GHz. Therefore any amplifier operating at those frequencies would require both wide bandwidth and the highest possible gain.

To achieve amplification with Si based technologies around $f_{max}/2$ and above, SiGe HBT [4]–[7] and CMOS [8], [9] technology based amplifiers are implemented using various gain-boosting techniques. In [10] and [11], LNA was implemented with two different circuit topologies but without any gain-boosting technique at frequency below $f_{max}/2$. Only [5] has implemented the amplifier at frequency as high as $2/3(f_{max})$ using gain-boosting technique. However, it doesn't mention the impact of gain-boosting on the noise performance of the amplifier.

This low noise amplifier operates at frequency as high as $2/3(f_{max})$ without any gain-boosting technique in 130 nm SiGe BiCMOS. The LNA uses four stages of pseudo differential cascode topology which measures 12.9 dB of gain at center frequency 290 GHz and 11.2 dB at 300 GHz. LNA also provides wideband frequency response of 23 GHz. To the authors' knowledge, this LNA achieves, without any gain-boosting technique, the highest gain at $2/3(f_{max})$ in SiGe technology.

II. LNA Circuit Design

A. Technology, Transistor selection and Modeling

The circuit is designed with IHP SG13G2 SiGe BiCMOS process with f_t/f_{max} of 300 GHz/450 GHz. Each bipolar transistor in the LNA circuit has emitter area of 4×0.9×0.07 um^2. The BEOL of the process consists of seven Al layers with two thick top layers and metal-insulator-metal (MIM) capacitor between TM1 and M5 with 1.5 fF/um^2 density. For circuit simulations, Vertical Bipolar Inter Company Model (VBIC) and High Current Model (HICUM) models of SiGe HBT are available. The entire design is simulated with VBIC model of SiGe HBT.

B. Circuit Design

As shown in Fig. 1, LNA consists of four stages and each stage has pseudo-differential cascode topology. Common emitter part of cascode topology offers better noise performance and common base offers good gain along with better isolation. Each HBT in four stages of LNA is biased at an I_c of 8.5 mA which gives, in simulation, 14 dB gain with 16 dB of noise figure.

Differential input of the first stage and output of the last stage are converted to single ended 50 ohm line using a Marchand balun. Input and output impedance matching is achieved using both L-shaped LC network and tuned GSG pads. Passive structure of the matching network is kept simple to minimize losses at higher frequencies. LC network is implemented with the 4 um wide transmission line and MIM capacitors. Length of transmission lines (TL1 and TL2 = 34 μm, TL5 and TL6 = 30 μm) and MIM capacitors (C1 and C2 = 6 fF, C6 and C7 = 5 fF) are tuned to perform the impedance matching of the first stage of the LNA. The other stages are designed similarly. However, these are tuned at slightly different frequencies using different inter-stage LC networks. Load of each stage is designed with inductive C-shaped center-tapped transmission line (width = 2 μm) with equal length (TL3, TL4 = 26 μm) for all stages. Along with the LC network, 7 μm wide short circuit stubs, with length (TLS1, TLS2 = 46 μm), are used to tune out the pad capacitances of the input and output pads which helps in input and output matching of the LNA. This also provides some ESD protection, grounding all low-frequency interference. AC

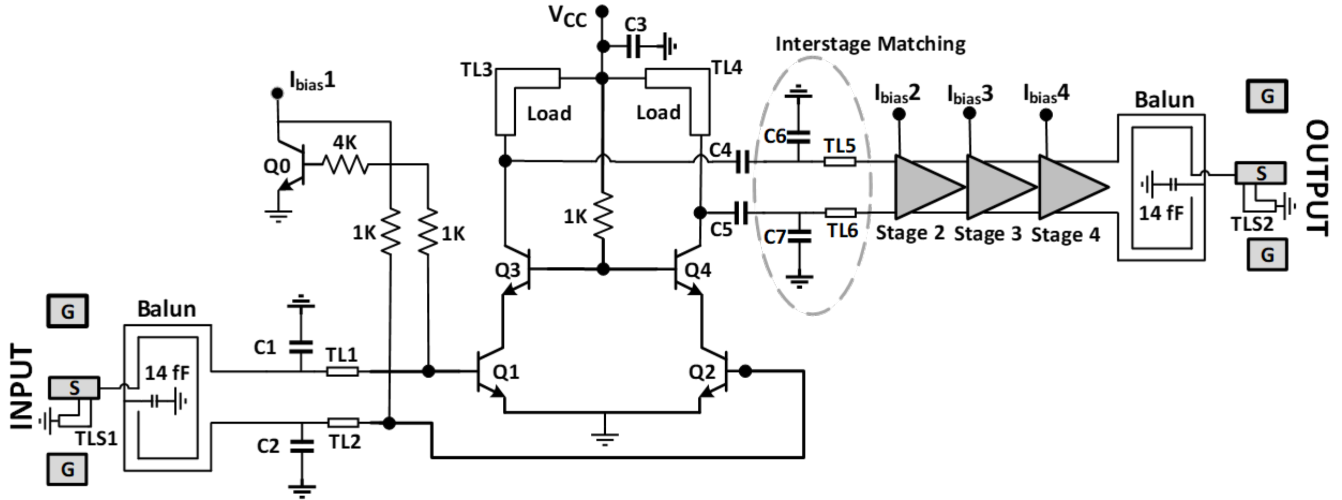


Fig. 1. Simplified schematic of the 4-stage LNA.

coupling capacitors (C4, C5 = 10 fF) of the same value are placed at the output of each stage. All passive components, including interconnects of the transistors, are simulated using Momentum solver of ADS which is 2.5D planar EM-simulator from Keysight Technologies.

All simulation and measurement results in this paper include pads. In simulations, input and output pad-balun combination losses are approximately 2.5 dB on both sides, respectively. As a part of a complete receiver, with differential on-chip antenna and on-chip interface to the following RF stages, losses can be avoided as baluns shown in Fig.1 are not part of the matching structure.

C. *Pads and Baluns*

As shown Fig. 2, the Marchand balun is implemented with edge-coupled asymmetric coupled lines using top layer (TM2) metal lines. Rectangular shaped inner ring and outer ring, having width of 2 μm and 4 μm respectively, are separated by gap of 2 μm. Outer ring of the balun is shorted to the ground using coupling capacitor of 14 fF. 3D diagram in Fig. 2 also depicts that the balun is combined with ground-signal-ground (GSG) pads where pad capacitor, formed by top metal (TM2) and lower metal (M2) layer, is resonated away with a short stub to improve the impedance matching. Insertion loss of combined structure is less than 2.5 dB over frequency range 260 GHz to 320 GHz with amplitude and phase imbalance less than 1 dB and 0.5 degree, respectively.

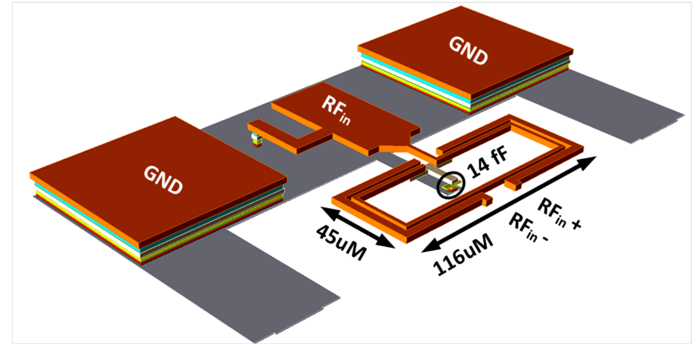


Fig. 2. Layout of the resonated GSG pad and Marchard balun.

III. Measurement Setup

LNA is characterized using VDI WR3.4 extenders connected to the vector network analyzer (VNA, Keysight PNA-X N5222B). The S-parameter measurement setup is shown in Fig. 3(a). Here, an external waveguide attenuator (VA-010E/G from Elmika UAB) is used to control signal levels during the measurements. The transmit (TX) frequency extender could measure also reflected power (S_{11}), and the LNA was rotated for the S_{12} and S_{22} measurements. A 6.5 dB insertion loss for the probe was measured at 290 GHz.

The compression point measurement of LNA was performed with a measurement setup shown in Fig. 3(b). Spectrum analyzer is connected to the output port of the receive (RX) frequency extender and it measures the IF signal at 279 MHz. The external waveguide attenuator was connected in this case to the input of RX frequency extender to avoid compression of the extender. The insertion losses of the RX frequency extender and the external waveguide attenuators were evaluated by comparing the measured output power of the TX extender measured by a power meter (Erickson Power Meter PM5B) to the reading of the spectrum analyzer (Keysight E4446A).

IV. Measurement Results

Microphotograph of the chip is shown in Fig. 4. The overall area is 532 $\times$ 462 um^2 and the active area without pads and baluns is 254 $\times$ 64 um^2.

A comparison of the simulated and measured S_{21} and S_{12} results are shown in Fig. 5(a). The LNA measures 12.9 dB of gain at center frequency 290 GHz and 11.2 dB at 300 GHz. The gain peak matches well with the simulations, but the

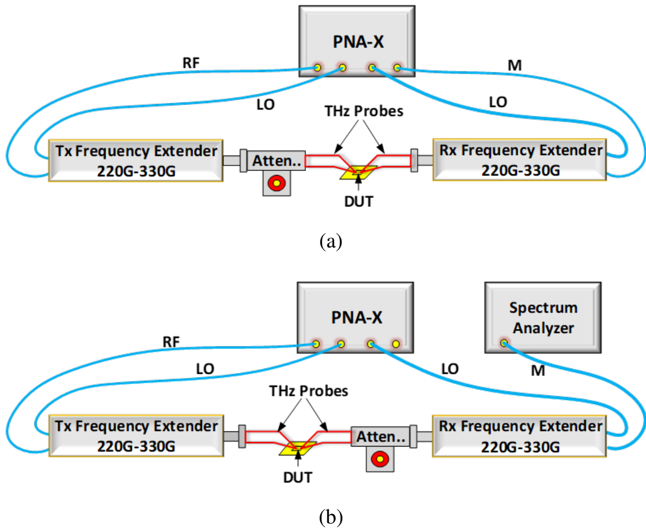


Fig. 3. Block diagrams of (a) S-parameters and (b) compression point measurements.

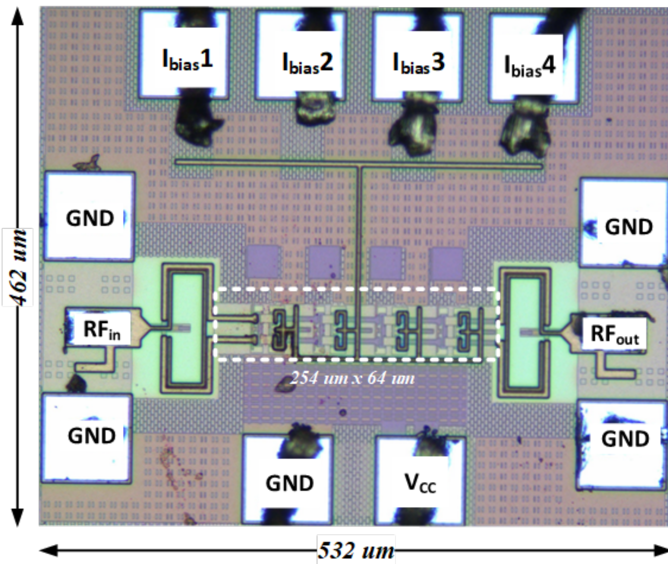
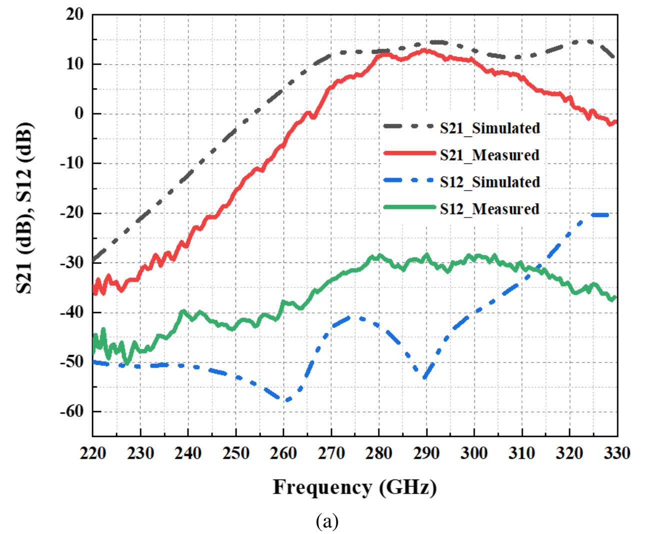


Fig. 4. Die micrograph of the LNA.



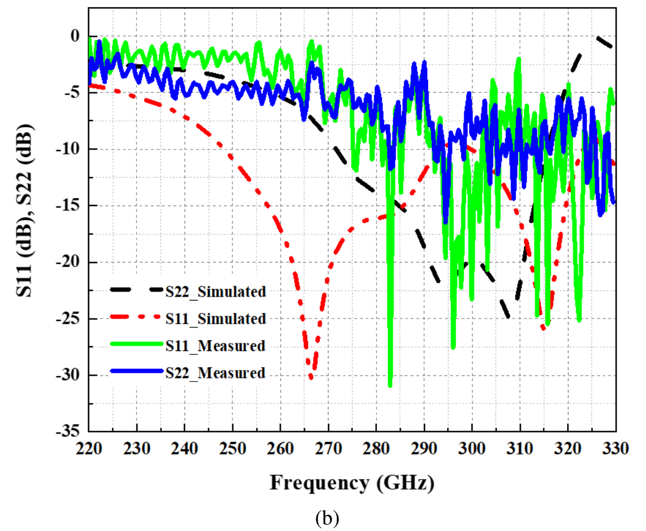


Fig. 5. Simulated and Measured S parameters: (a) Gain; (b) Reflection coefficients.

distributed resonances at 270, 290, and 325 GHz are merged, narrowing the measured passband width from the simulated. The S_{12} is at a low level, as expected in a multi-stage amplifier - it mostly depicts the coupling via supplies and across the chip. As EM-simulation of the entire LNA circuit as a one block was not feasible the circuit was divided into EM-simulated blocks of each stage of LNA with pads and balun as a separate EM-simulated block. Consequenctly, EM-simulation of LNA doesn't take into account all possible mutual coupling of EM-simulated blocks which probably explains the discrepancies between simulated and measured gain of the LNA. The simulated and the measured S_{11} and S_{22} are shown in Fig. 5(b). The designed matching resonances are not very well visible in the measurement results, but the overall matching of the implemented LNA is decent.

Figure 6 shows the compression behavior of the implemented LNA at 290 GHz. The external waveguide attenuator was set at 33.9 dB attenuation to guarantee a linear operation of the RX extender. The power level sweep at the LNA input was performed by altering the RF input level of the TX extender. Due to non-linear and steep slope of the power control caused by the extender specific care was applied when defining the input power level during the measurement. The reported input and output power levels in Fig. 6 are defined at the measurement probe tips. The 1 dB compression point of the LNA is -9.0 dBm based on curve shown in Fig. 6. The linear operation range of the LNA was partly limited due to the TX power control method of the measurement system.

Table 1 shows the comparison with state-of-the-art 130 nm SiGe BiCMOS amplifiers. This LNA clearly achieves broadband operation and the highest gain by far, operating at 290 and 300 GHz, that is near $2/3(f_{max})$ without any gain-boosting technique.

Table 1. Summary of the important performance parameters and comparison with related works

	This work	[4]	[5]	[6]	[7]	[10]	[11]
Technology	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe
f_t/f_{max} (GHz)	300/450	300/550	220/280	350/550	300/450	300/500	300/500
Frequency (GHz)	290	252	173	275	233	245	245
Topology	CC[a], Diff. (4 stages)	CC[a], Diff. (3 stages)	CE[b], SE[c] (3 stages)	Common Base (8 stages)	CC[a], Diff. (4stages)	CC[a], Diff. (5 stages)	Common Base (4 stages)
Gain Boosting Technique	No	Yes	Yes	Yes	Yes	Yes	No
Gain (dB)	12.9	21.5	18.5	10	22.5	18	12
3-dB BW (GHz)	23	11	8.2	7	10	8	25
NF (dB)	16 (Simulated)	-	-	18 (Simulated)	12.5 (Simulated)	11 (Measured)	11.3 (Simulated)
Input-Referred P_{1dB} (dBm)	-9.0	-20	-10	-10	-	-	-
P_{diss} (mW)	136	149	42	122.7	68	303.4	28
Area (um^2)	532 X 462	580 X 290	865 X 465	1065 X 355	280 X 270	360 X 430	420 X 460

[a] Cascode. [b] Common Emitter. [c] Single Ended.

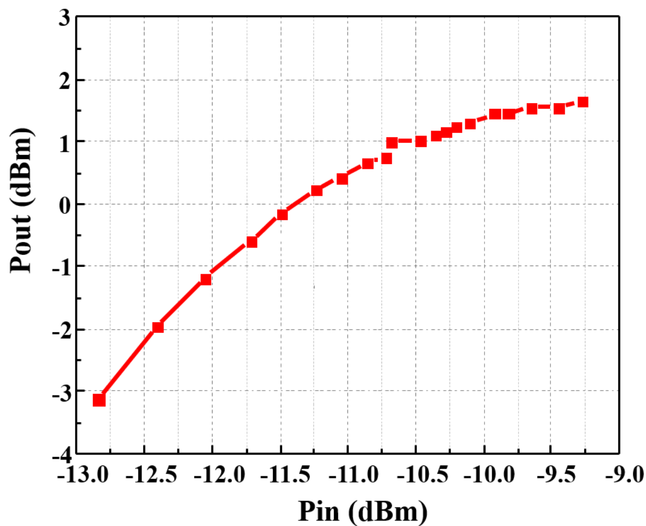


Fig. 6. Measured compression gain curve of implemented LNA at 290 GHz.

V. Conclusion

A LNA operating at 290 GHz is successfully implemented in 130 nm SiGe BiCMOS technology with f_t/f_{max} of 300 GHz/450 GHz. The LNA is designed, without any gain boosting technique, near $2/3(f_{max})$ and it measures 12.8 dB and 11.2 dB of small signal gain at 290 GHz and 300 GHz, respectively. This indicates potential for the use in receivers at sub-THz and THz regions in future high speed communication system like 6G. To authors' best knowledge, this LNA achieves the highest gain, without any gain boosting technique, in that particular technology at frequency beyond $f_{max}/2$.

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