FPGA Implementation of Stair Matrix based Massive MIMO Detection

Shahriar Shahabuddin*, Mahmoud A. Albreem*‡, Mohammad Shahanewaz Shahabuddin†,
Zaheer Khan*, Markku Juntti*
*Centre for Wireless Communications, University of Oulu, Finland
‡A'Sharqiyah University, Oman
†Vaasa University of Applied Science, Finland
Email: *[firstname.lastname]@oulu.fi, †e1900302@vamk.fi, ‡[firstname.lastname]@asu.edu.om

Abstract—Approximate matrix inversion based methods is widely used for linear massive multiple-input multiple-output (MIMO) received symbol vector detection. Such detectors typically utilize the diagonally dominant channel matrix of a massive MIMO system. Instead of diagonal matrix, a stair matrix can be utilized to improve the error-rate performance of a massive MIMO detector. In this paper, we present very large-scale integration (VLSI) architecture and field programmable gate array (FPGA) implementation of a stair matrix based iterative detection algorithm. The architecture supports a base station with 128 antennas, 8 users with single antenna, and 256 quadrature amplitude modulation (QAM). The stair matrix based detector can deliver a 142.34 Mbps data rate and reach a clock frequency of 258 MHz in a Xilinx Virtex-7 FPGA. The detector provides superior error-rate performance and higher scaled throughput than most contemporary massive MIMO detectors.

Index Terms—Massive MIMO, approximate matrix inversion, stair matrix, Gauss Seidel, Neumann Series, MIMO detection, FPGA, VLSI.

I. INTRODUCTION

Massive multiple-input multiple-output (MIMO) is a key technology for fifth generation (5G) systems to enhance spectral and energy efficiency, coverage and mobility within the available radio spectrum. Massive MIMO is the successor of conventional small-scale MIMO, where the number of antennas at the base station (BS) and the number of users is relatively high [1]. Despite all the benefits of massive MIMO, the technology also suffers from higher computational complexity. MIMO detection in the uplink is one of the most complex part of a massive MIMO BS due to the increasing number of users and BS antennas. The complexity of massive MIMO detectors increase so rapidly that conventional exact inversion-based linear massive MIMO detection might be too complex for certain BS products. In consequence, a new class of detectors based on approximate inversion based methods have become a popular choice among the large-scale integration (VLSI) community over the past decade. Approximate inversion based detectors are based on the principle that for certain antenna configurations, the equalization matrix of linear detection is diagonally dominant. Several approximate inversion based detectors, which utilize a diagonal matrix can be found in the literature, such as Neumann series approximation (NSA) [2], Gauss Seidel (GS) [3], conjugate gradient (CG) [4], Richardson method [5] etc.

Instead of diagonal matrix, a stair matrix can be utilized for massive MIMO detection [6]. With a small additional complexity, the stair matrix based detectors can accelerate convergence rate of an approximate inversion based detectors, such as NSA. In addition, a stair matrix can also be used to develop novel low-complexity massive MIMO detection methods. In this paper, we propose FPGA implementation for such a stair matrix based detection method. We present simulation results to demonstrate superior error-rate performance of stair matrix based detection and also determine necessary word length for the circuit. We develop an iterative and time-shared architecture for the detector using VHSIC Hardware Description Language (VHDL) and mapped on a Xilinx Virtex-7 FPGA. The architecture supports a base station with 128 antennas, 8 users and 256 quadrature amplitude modulation (QAM). The stair matrix based detector provides 142.34 Mbps detection rate at a 258 MHz clock frequency. The rest of the paper is organized in the following way: In Section II, a massive MIMO system and detection methods are discussed. In Section III, the stair matrix based detection algorithm and its complexity is presented. Fixed and floating-point performance of the detector are presented in Section IV. Proposed VLSI architecture and FPGA implementation are presented in Section 3 and VI, respectively. The conclusion is drawn in Section VII.

II. SYSTEM MODEL AND DETECTION METHODS

We assume, a total of U single antenna users are transmitting towards a massive MIMO BS with N antennas, where $U \leq N$. Assuming a frequency flat channel between the users and BS, the transmit and receive vector relationship can be characterized as

$$\mathbf{y} = \mathbf{Hx} + \mathbf{n}, \tag{1}$$

where $\mathbf{y} \in \mathbb{C}^B$ is a received signal vector, $\mathbf{x} \in \mathbb{C}^U$ is a transmit symbol vector, $\mathbf{H} \in \mathbb{C}^{B \times U}$ is a channel matrix, and $\mathbf{n} \in \mathbb{C}^B$ is a circularly symmetric complex white Gaussian noise vector with zero mean and σ^2 noise variance. In Fig. 1, a massive MIMO system model is presented.

The task of a MIMO symbol detector is to determine the transmitted symbol vector $\mathbf{x}$ from the received signal vector $\mathbf{y}$. Two recurrent linear detection methods are based on zero-forcing (ZF) and linear minimum mean-square error (MMSE)
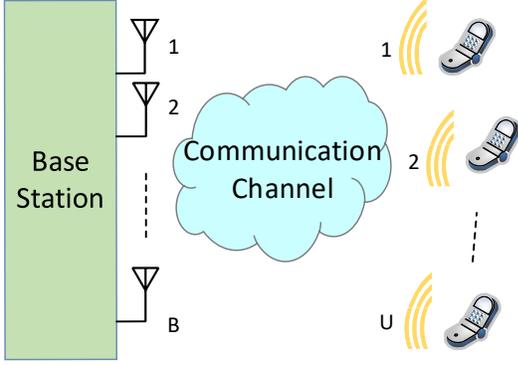
Fig. 1: Massive MIMO system model.

equalization. ZF inverts the channel matrix $\mathbf{H}$ to determine the transmitted vector and does not consider the effect of noise vector $\mathbf{n}$, which can be expressed as

$$\tilde{\mathbf{x}}_{\text{ZF}} = \mathbf{H}^\dagger \mathbf{y} = (\mathbf{H^H H})^{-1} \mathbf{H^H y}, \qquad (2)$$

where $\mathbf{H}^\dagger$ is a pseudo-inverse of $\mathbf{H}$. The ZF detector requires an inversion of the *Gramian* matrix, $\mathbf{G}$, where $\mathbf{G}_{\text{ZF}} = \mathbf{H^H H}$. The MMSE detector takes noise into account and provides better performance than ZF. MMSE detection can be expressed as

$$\tilde{\mathbf{x}}_{\text{MMSE}} = (\mathbf{H^H H} + \sigma^2 \mathbf{I}_U)^{-1} \mathbf{H^H y}, \qquad (3)$$

where $\mathbf{I}_U$ is the $U \times U$ identity matrix. The *Gramian* matrix is modified with a regularization by noise variance for MMSE, i.e., $\mathbf{G}_{\text{MMSE}} = \mathbf{H^H H} + \sigma^2 \mathbf{I}_U$.

For small-scale MIMO detection, the inversion of a *Gramian* was based on exact matrix inversion methods. However, the exact inversion can be complex as the number of users increases. For example, *Gramian* of a 16 users system ($U = 16$) will be a 16×16 matrix. Therefore, the approximate inversion based detection methods are usually used by the VLSI community. These detection mechanisms are iterative and they heavily utilize the diagonal matrix. For example, in GS method, $\mathbf{G}$ is decomposed as

$$\mathbf{G} = \mathbf{D} + \mathbf{L} + \mathbf{R}, \qquad (4)$$

where $\mathbf{D}$, $\mathbf{L}$ and $\mathbf{R}$ are the diagonal component, the strictly lower triangular component, and strictly upper triangular component, respectively. The GS can be used to estimate the transmitted signal vector $\hat{\mathbf{x}}$ as

$$\hat{\mathbf{x}}_t = (\mathbf{D} + \mathbf{L})^{-1} (\hat{\mathbf{x}}_{\text{MF}} - \mathbf{R}\hat{\mathbf{x}}_{t-1}), \qquad (5)$$

where $\hat{\mathbf{x}}_{\text{MF}} = \mathbf{H}^H \mathbf{y}$ is a matched filter [3].

III. Stair Matrix based Gauss-Seidel Method

A stair matrix is a special tri-diagonal matrix where the off-diagonal elements on either the even or the odd row are zeros [6]. Matrix $\mathbf{S}$ is considered as a stair matrix if one of the following conditions is satisfied:

- $\mathbf{S}_{(i,i-1)} = 0, \mathbf{S}_{(i,i+1)} = 0$ where $i = 2, 4, ..., 2\left\lfloor \frac{K}{2} \right\rfloor$
- $\mathbf{S}_{(i,i-1)} = 0, \mathbf{S}_{(i,i+1)} = 0$ where $i = 1, 3, ..., 2\left\lfloor \frac{K-1}{2} \right\rfloor + 1$

Algorithm 1 Inversion of a Stair Matrix

input: $\mathbf{S}$
outputs: $\mathbf{S}^{-1}$
1: **for** $i = 1 : 1 : U$
2: $\quad \mathbf{S}_{i,i}^{-1} = 1/\mathbf{S}_{i,i}$
3: **end**
4: **for** $i = 2 : 2 : 2\lfloor U/2 \rfloor$
5: $\quad \mathbf{S}_{(i,i-1)}^{-1} = -\mathbf{G}_{(i,i-1)}\mathbf{S}_{i,i}^{-1}\mathbf{S}_{(i-1,i-1)}^{-1}$
6: $\quad \mathbf{S}_{(i,i+1)}^{-1} = -\mathbf{G}_{(i,i+1)}\mathbf{S}_{i,i}^{-1}\mathbf{S}_{(i+1,i+1)}^{-1}$
7: **end**

TABLE I: Complexity comparison

Algorithm	Computational complexity
CG	$(K+1)(4U^2 + 20U)$
NSA	$(K-1)(2U^3 + 2U^2 - 2U)$
GS	$6KU^2$
Stair Matrix	$K(4U^2 - 2U)$

The stair matrix $\mathbf{S}$ is essentially a diagonal matrix $\mathbf{D}$ with some additional off-diagonal elements. A 6×6 stair matrix can be expressed with either of the following forms:

$$\mathbf{S} = \begin{bmatrix} \times & \times & & & & \\ & \times & & & & \\ & \times & \times & \times & & \\ & & & \times & & \\ & & & \times & \times & \times \\ & & & & & \times \end{bmatrix} \quad \text{or} \quad \mathbf{S} = \begin{bmatrix} \times & & & & & \\ \times & \times & \times & & & \\ & & \times & & & \\ & & \times & \times & \times & \\ & & & & \times & \\ & & & & \times & \times \end{bmatrix}$$

The stair matrix $\mathbf{S}$ can be extracted from the *Gramian* by only extracting the cross shaped values shown here. The inversion of a stair matrix can be calculated in a straightforward manner, which is presented in Algorithm 1. The diagonal elements are computed with reciprocals and the off-diagonal elements require a couple of multiplications. An iterative detection method based on stair matrix is proposed in [6]. In their proposed method, the initial solution is based on inverse of stair matrix and matched filter.

$$\hat{\mathbf{x}}_{(0)} = \mathbf{S}^{-1}\hat{\mathbf{x}}_{\text{MF}}. \qquad (6)$$

This solution is updated with each iteration in the following way:

$$\hat{\mathbf{x}}_t = \mathbf{S}^{-1} ((\mathbf{S} - \mathbf{G})\hat{\mathbf{x}}_{t-1} + \hat{\mathbf{x}}_{\text{MF}}) \qquad (7)$$

It is evident that the solution only requires an inversion of the stair matrix, which is already presented in Algorithm 1. The rest of the algorithm requires a matrix inversion and addition with matched filter. The stair matrix based detection method requires a total of U number of divisions and $t(4U^2 - 2U)$ number of real multiplications. In Table I, the complexity of the stair matrix based detection algorithm is compared to three most popular approximate inversion based detection methods. The comparison is based on the number of real multiplication required for each detection mechanism. It is evident from the table that stair matrix based detection method is less complex than most approximate inversion based detectors.

IV. SIMULATION RESULTS

We present error-rate performance of different detection mechanism in Fig. 2. We simulate NSA, GS, MMSE, CG and Richardson methods to compare with the stair matrix based detection. Here, we used 10,000 Monte-Carlo trials for all simulations. The modulation scheme for these simulations is 256-QAM. We consider an i.i.d. Rayleigh fading channel between the BS and users. In Fig. 2, we simulate the detectors for 8 users transmitting to a BS equipped with 128 antennas. The number of iterations used for all the algorithms is $t = 2$. GS and stair matrix based detectors reach near MMSE performance for this scenario. The stair matrix based detector outperforms NSA, Richardson and CG methods by a significant margin.
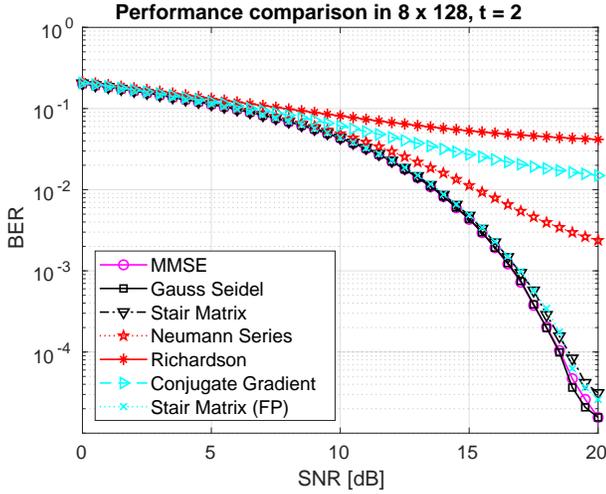

Fig. 2: Detector performance for 128 BS antennas and 8 users with 256-QAM.

We also present the fixed-point simulation performance of stair matrix in Fig. 2. We curve of the stair matrix based detector with fixed word lengths is denoted by FP. The Gramian matrix is set to a total of 12 bits with 8 bits for fraction, while the matched filter inputs are set to a total of 15 bits with 10 bits of fraction. The output of the inverse of $\mathbf{S}$ is set to 17 bits. The outputs of multiplication between $(\mathbf{S} - \mathbf{G})$ and $\hat{\mathbf{x}}$ are set to 20 bits with 16 bits of fraction. The values of $\hat{\mathbf{x}}$ are set to 12 bits with 8 bits of fraction in the entire simulation. These optimal word lengths are found after numerous simulations in the Matlab environment. Wrapping and rounding mechanisms are used in the simulations for quantizing the integer and fractional parts, respectively. Fig. 2 shows that the fixed-point version of a stair matrix based detector coincides with its floating-point counterpart.

V. VLSI ARCHITECTURE

We present an iterative and time-shared VLSI architecture for the stair matrix based massive MIMO detection. The VLSI architecture is designed for maximum utilization of a complex multiplier array, which is the crux of the detector operation. A VLSI architecture based on a systolic array with numerous multiply-and-accumulate (MAC) processing elements (PE) is another candidate for such a detector. However, we prefer the proposed time-shared architecture due to the iterative nature of our algorithm.

A high level block diagram of the proposed VLSI architecture is presented in Fig. 3. We assume the *Gramian* and matched filters are computed during pre-processing stage and we focus only on the detection part in this paper. The inputs of the architecture comes from subtraction of the stair matrix from the *Gramian* matrix ($\mathbf{S} - \mathbf{G}$), diagonal elements of ($\mathbf{G}$), non-diagonal elements ($\mathbf{G}$), and matched filter. A 13 bits input where 9 bits are fraction is used for $\mathbf{G}$ matrix. Even though 12 bits are sufficient for $\mathbf{G}$ according to Fig. 2, we relax the word length by one bit to avoid any unexpected quantization errors. The memory part is depicted in green, while the logic parts in blue in Fig. 3. It should be noted that the size of the blocks in Fig. 3 is not proportional to the actual area they occupy in the FPGA die.
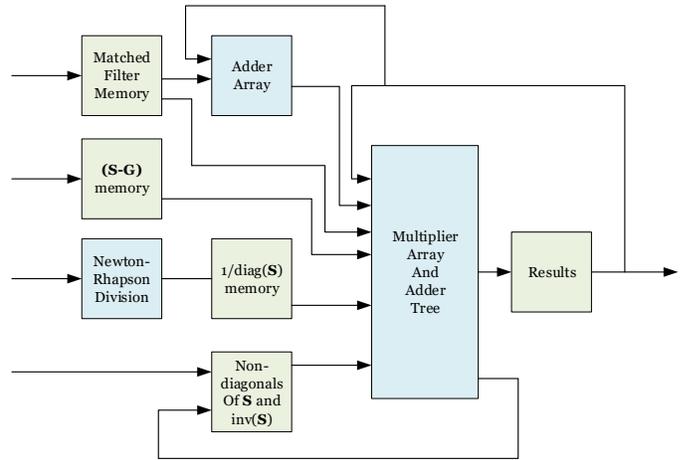

Fig. 3: High level architecture of the VLSI architecture for stair matrix based detection.

According to Fig. 2, the entire architecture can be divided in four major parts: (1) a Newton-Raphson divider, (2) a multiplier array, (3) an adder tree and an adder array, and (4) control logic. The main memories involved with the architecture is related to $\mathbf{S} - \mathbf{G}$, and register arrays to store incoming matched filter, diagonal and non-diagonals of $\mathbf{S}^{-1}$, and an array at the output. We require to store 64 elements of $\mathbf{S} - \mathbf{G}$ because the Gramian becomes 8×8 for an 8 users massive MIMO system. We use a memory which stores 8 elements of $\mathbf{S} - \mathbf{G}$ in each address to utilize the multiplier array properly. Thus, each word in the memory is 26×8 bits wide. However, the values of $\mathbf{S} - \mathbf{G}$ is assumed to be written one at a time, and therefore, we require a separate register array and associated logic to concatenate the 8 elements into a longer word of 26×8 bits and write into the $\mathbf{S} - \mathbf{G}$ memory. A few points to be noted here: (1) $\mathbf{S} - \mathbf{G}$ do not require any subtraction, because the non-zero elements of $\mathbf{S}$ comes straight away from $\mathbf{G}$, and the subtraction output will be zero for those elements. (2) Due to the symmetric nature, it is possible to store only the upper or lower triangular part of $\mathbf{G}$. However,

writing and reading from a triangular memory will require more complex logic. (3) We assume the chip select, write enable, write address and write data comes as an input to the architecture.

During first 64 cycles required to load the $\mathbf{S} - \mathbf{G}$ memory, we compute the inverse of the diagonal elements with Newton-Raphson method [7]. The inverse $1/x$ can be computed in an iterative manner with Newton-Raphson method as

$$x_{k+1} = 2x_k - xx_k^2, \tag{8}$$

where k is the number o iterations. The initial value x_0 follows the convergence criterion $0 < x_0 < 2/x$. The initial values are typically stored in a look-up table (LUT). To control the dynamic range, a shift operation is applied on x. This shift operation ensures that the result lies in the range of $[1/2, 1]$. We use a 18 bit divider and store $\mathrm{diag}(\mathbf{G})$ in a register array.

The non-diagonal elements of $\mathbf{S}$ are stored in a separate register array. To our convenience, we only have a total of seven non-zero non-diagonal values of in a 8×8 stair matrix. The corresponding non-zero elements of $1/\mathbf{S}$ can be computed with only two multiplications according to Algorithm 1. We store the non-diagonal elements of $1/\mathbf{S}$ in a separate register array. The main computation unit of the architecture is built upon an array of eight complex multipliers and an adder tree. As complex multipliers are costly, we re-use them in a time shared manner to compute (1) initial value of $\hat{\mathbf{x}}$, (2) matrix $(\mathbf{S} - \mathbf{G})$ and vector $\hat{\mathbf{x}}$ multiplication, (3) to compute non-diagonal elements of $1/\mathbf{S}$ and (4) the final multiplication required between $\mathbf{S}^{-1}$ and $((\mathbf{S} - \mathbf{G})\hat{\mathbf{x}}_{t-1} + \hat{\mathbf{x}}_{\mathrm{MF}})$.

VI. FPGA Implementation and Comparison

The VLSI architecture is developed with VHDL on register-transfer level (RTL) and mapped on a Xilinx Virtex-7 XC7VX690T FPGA. For synthesis and implementation strategy, Vivado default settings is used. The default mode is selected for the -flatten_hierarchy option in Vivado design tool to keep the same top level hierarchy after synthesis. A total of 116 cycles are required to complete the two iterations of the stair matrix based detector, where 25 cycles are required for each iteration of the algorithm. The architecture can reach 258 MHz of maximum clock frequency. Therefore, the 8 users system can reach upto 142.34 Mbps throughput. Several such VLSI circuits working in parallel on different orthogonal frequency division multiplexing (OFDM) tone can increase the throughput to Gbps, which is required for 5G systems.

In Table II, we compare our FPGA implementation with NSA implementation of [2] and GS implementations of [3] and [8]. The NSA detector takes a significant amount of LUT and FF slices compared to other implementations and able to reach a high throughput value even after $t = 3$ iterations. As the implementation also takes a significant area, the NSA implementations provide lower scaled throughput compared to our implementation. The GS implementations are both provided for $t = 1$ iterations. The GS implementation of [3] provides lower throughput as well as lower scaled throughput compared to our implementation. The throughput

TABLE II: Comparison of FPGA implementations for 8 users massive MIMO detectors

Detection algorithm	Stair Matrix	NSA [2]	GS [3]	GS [8]
Modulation Scheme	256-QAM	64-QAM	64-QAM	64-QAM
Iteration	2	3	1	1
LUT slices	16211	148797	18976	17944
FF slices	15793	161934	15864	19750
DSP	112	1016	232	274
Clock freq. [MHz]	258	317	309	352
Throughput [Mbps]	142.34	621	48	127
Throughput/slices[a] (Mbps/K slices)	4.4481	2.0032	1.4118	3.4324

[a] Summation of LUT and FF slices.

will be further reduced for $t = 2$ iterations which we have used in our Matlab simulations of Fig. 2. The improved GS architecture proposed in [8] provides higher scaled throughput than that of [3]. However, the scaled throughput is still lower than our implementation and [8] also used only $t = 1$ iterations for their result.

VII. Conclusion

In this paper, we proposed a VLSI architecture and FPGA implementation of a stair matrix based massive MIMO detection algorithm. The algorithm provides satisfactory performance when the ratio between the numbers of BS antennas and users is high. We presented the fixed-point simulations to find the optimal word lengths for our architecture. The implementation reaches a maximum clock frequency of 258 MHz and provides 142.34 Mbps. The architecture provides reasonably higher throughput and better error-rate performance than most other massive MIMO detectors. Thus, the proposed detector is an attractive solution for 5G BS receiver implementation..

References

[1] M. A. Albreem, M. Juntti, and S. Shahabuddin, "Massive MIMO Detection Techniques: A Survey," *IEEE Communications Surveys Tutorials*, vol. 21, no. 4, pp. 3109–3132, 2019.

[2] M. Wu, B. Yin, G. Wang, C. Dick, J. Cavallaro, and C. Studer, "Large-scale MIMO detection for 3GPP LTE: Algorithm and FPGA implementation," *IEEE Journal of Selected Topics in Signal Processing*, vol. 8, no. 5, pp. 916–929, Oct. 2014.

[3] Z. Wu, C. Zhang, Y. Xue, S. Xu, and X. You, "Efficient architecture for soft-output massive MIMO detection with Gauss-Seidel method," in *IEEE International Symposium on Circuits and Systems*, May 2016, pp. 1886–1889.

[4] S. Shahabuddin, M. S. Islam, M. S. Shahabuddin, M. A. Albreem, and M. Juntti, "Matrix Decomposition for Massive MIMO Detection," in *IEEE Nordic Circuits and Systems Conference*, Oct. 2020.

[5] X. Gao, L. Dai, C. Yuen, and Y. Zhang, "Low-complexity MMSE signal detection based on Richardson method for large-scale MIMO systems," in *IEEE Vehicular Technology Conference*, 2014, pp. 1–5.

[6] F. Jiang, C. Li, Z. Gong, and R. Su, "Stair matrix and its applications to Massive MIMO uplink data detection," *IEEE Transactions on Communications*, vol. 66, no. 6, pp. 2437–2455, 2018.

[7] S. Shahabuddin, J. Janhunen, Z. Khan, M. Juntti, and A. Ghazi, "A customized lattice reduction multiprocessor for MIMO detection," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 2976–2979.

[8] J. Zeng, J. Lin, and Z. Wang, "An improved Gauss-Seidel algorithm and its efficient architecture for massive MIMO systems," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 9, pp. 1194–1198, 2018.