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Suppression of dynamic current leakage in avalanche *S*-diode switching circuits

Ilya A. Prudaev, Sergey N. Vainshtein, Viktor V. Kopyev, Vladimir L. Oleinik, and Sergey N. Marochkin

***Abstract*—This work investigates the dynamic current leakage of *S*-diode, which is a GaAs-based avalanche switch doped with deep Fe acceptor traps. The dynamic leakage has negative effect on superfast switching parameters of this unique device, and here we suggest an original way of reducing the leakage by means of circuit design. It is shown that an additional bias for avalanche S-diode in the current pulse generation circuit forms a negatively charged layer of iron traps near the electron-injecting junction. As a result, the concentration of nonequilibrium electrons goes down, which leads to a decrease in leakage current by ~ 3-4 times, and a rise in S-diode switching voltage. The results were obtained in the experimental study and are approved by calculation.**

***Index Terms*—Avalanche breakdown, Diodes, Microwave switches, Pulse power systems, Closing switches**

I. Introduction

An avalanche *S*-diode is a semiconductor closing switch with *S*-shaped current-voltage characteristics (*I*-*V* curve). Avalanche diodes can commutate high voltage in less than 1 ns [1, 2]. The most probable mechanism to provide *S*-diode switching is the collapsing field domains (CFD) [3, 4] when switching occurs in local areas (filaments with current density of 1-10 MA/cm^2) [5]. With its small-sized current channels, the avalanche *S*-diode is a miniature device, thus being effectively used in circuits for generating nanosecond current pulses with an amplitude of tens of amperes [5]. In particular, such circuits are required for pumping semiconductor lasers for pulsed LiDARs [6, 7]. In such circuits, a pulsed voltage is supplied to the *S*-diode, resulting in a pre-switching leakage current [5]. Thus, before switching avalanche *S*-diodes in a dynamic mode, a parasitic current of 0.5-1 A flows through the load for 30-50 ns, which is an undesirable effect. The paper deals with a circuit design solution for reducing the said leakage and analyzes physical processes occurring in an avalanche *S*-diode.

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II. Experimental and Calculation Details

The structure of avalanche *S*-diodes under study is described in detail in [5]. The diodes were fabricated from GaAs structures obtained by vapor-phase epitaxy and doped with a deep Fe acceptor (ionization energy ΔE_{Fe} = 0.5 eV). Fig. 1 shows the doping profiles in this structure. Here, a forward-biased n^+-π junction injects electrons, while a reverse-biased π-n^0 junction injects holes in an avalanche breakdown mode. In a high-resistance π-layer, charge carriers are likely to be captured by deep Fe acceptors or emitted, which determines pre-switching current flow dynamics.

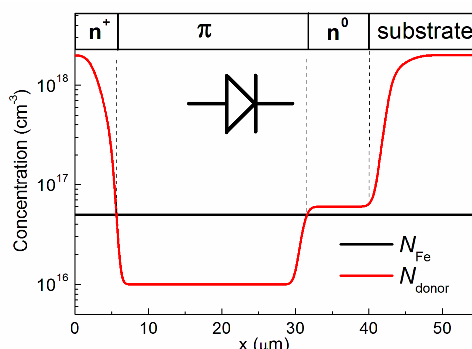

Fig. 1. Doping profiles across the *S*-diode structure. A sketch of the structure is shown at the top of the figure.

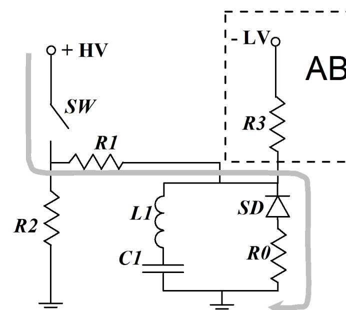

Fig. 2. Electrical circuit with additional bias (AB - circled with a dashed line): *R0* = 2.35 Ω, *R1* = 100 kΩ, *R2* = 30 Ω, *R3* = 1 kΩ, *C1* = 330 pF, *L1* = 12 nH, HV - high voltage source connection (up to 250 V), LV - low voltage source connection (up to 10 V), SW - transistor switch. Arrow shows parasitic (leakage) current direction.

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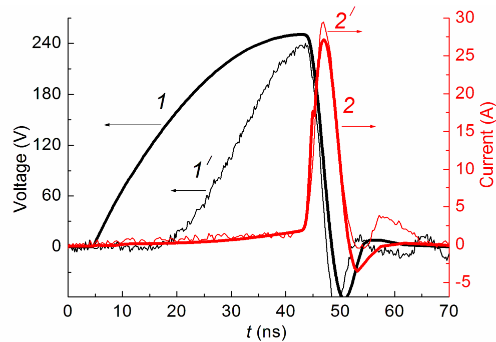

Fig. 3. Voltage across the *S*-diode (left axis) and current (right axis): $1^{/}$ - experimental voltage, $2^{/}$ - experimental current, 1 - calculated voltage, 2 - calculated current.

In the operating mode, a pulse voltage is supplied to the structure with a ramp of $dV/dt = 10^{10}$-10^{11} V/s using the circuit presented in Fig. 2 (without circuit of additional bias, AB). This brings about an intensive electron injection from the n^+-π junction and electron drift to the reverse-biased π-n^0 junction (like bipolar junction transistors, this mode can be characterized as a punch-through effect).

The experimental dependences of the avalanche *S*-diode voltage and the *R0* load resistance current on time are shown in Fig. 3 (curves $1^{/}$ and $2^{/}$, typical dependences for one *S*-diode). The measurements were taken at a frequency of 1 kHz (to exclude heating) using an oscilloscope with a bandwidth of 500 MHz. During switching, the voltage across the *S*-diode drops sharply, and a current pulse is formed on the load, with a shape caused by the reactance of the circuit (pulse width is $\tau \approx 2.1\cdot(L1\cdot C1)^{1/2}$, $L1$ = 12 nH, $C1$ = 330 pF). Fig. 3 shows that before switching (in the time interval of 5 ns < t < 43 ns, LV = 0 V), a current flows through the load due to a punch-through effect. Integration of curve $2^{/}$ within this interval gives a charge of 31 nC. Notably, as soon as the circuit reactance (*L1*, *C1*) reduces and a pulse starts to last 1 ns, this charge leakage will be comparable to a useful charge transferred to the load (29A·1 ns = 29 nC). Thus, eliminating this leakage should nearly double the efficiency of current pulse generators.

It has been experimentally found that an additional DC bias with a polarity reversed to the pulse voltage significantly reduces the leakage across the avalanche *S*-diode. In this case, it is enough to use the AB-circuit (cycled by the dashed line in Fig. 2). To analyze this effect, the Technology Computer-Aided Design (TCAD) Synopsys (Sentaurus) software was used for calculations. A 1D avalanche *S*-diode model was developed earlier through hydrodynamic approximation [5]. It relies on the switching of the semiconductor structure through the filament channel [4], the generation of CFDs [8], and the recharging of deep Fe traps [5]. The *S*-diode is simulated as a parallel connection of two channels: one corresponds to the entire area of the *S*-diode (1.5 mm^2), the other – to a small-area filament (300 μm^2). A reduced concentration of electron traps is set in the filament region, which provokes more intense electron injection and superfast switching [5]. A pre-switching leakage occurs over the entire area of the *S*-diode (in this paper, the current dynamics over the entire area is of interest).

The calculation results for this model are shown in Fig. 3 (bold lines 1 and 2). A good qualitative agreement between the calculated and experimental data suggests that the model can be applied to analyze physical processes occurring in the *S*-diode.

III. Results and Discussion

Fig. 4 shows the dynamic leakage region (current through the load versus pre-switching time) at different applied voltages LV. Based on the findings the higher the LV voltage the lower the leakage current, which is consistent with the experiment. Unfortunately, it is impossible to compare the calculated and experimental functional dependences of $I(t)$, since in the experiment the measured values are comparable in order of magnitude with the noise. Just the same, it is possible to compare the amount of charge flowing through the *S*-diode before switching (it is just enough to integrate the $I(t)$ dependences in the leakage region). The experiment shows that changing the LV voltage from 0 to -10 V reduces the leakage charge from 31 to 7 nC. The calculation gives similar values (from 28 to 9 nC).

The charge density and electric field profiles analyzed in the *S*-diode structure showed that the leakage decreases due to a negatively charged layer forming near the n^+-π junction. This layer prevents the injection of electrons and remains in the structure for a long time. Fig. 5 schematically shows the energy diagrams of structures in the pre-switching in n^+-π junction region. The higher the applied voltage LV, the wider the space charge region and the higher the barrier height (Φ) for injected electrons. Fig. 6 shows the distribution of charge density in the structure of the *S*-diode at different LV bias (at t = 0 in Fig. 4b). The negatively charged layer is located in the range of 6μm < x < 8μm and caused by electrons captured by deep Fe acceptor centers. The layer is formed during 1 ms before supplying the pulse voltage with a ramp of $dV/dt = 10^{10}$-10^{11} V/s. Unlike the conventional space charge region formed by a shallow acceptor impurity, this layer is disappearing for quite a long time.

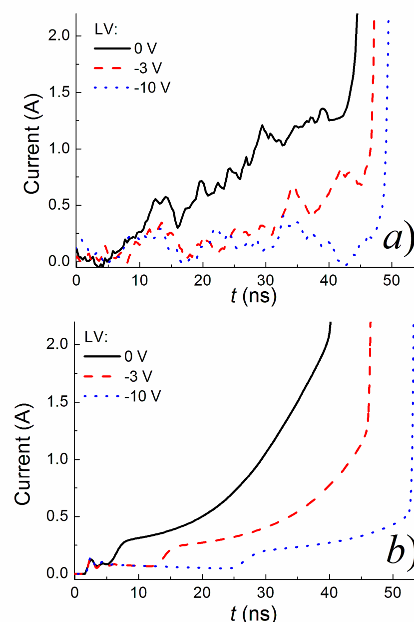

Fig. 4. (a) Experimental and (b) calculated current for three different voltages of LV supply in the region of dynamic current leakage.

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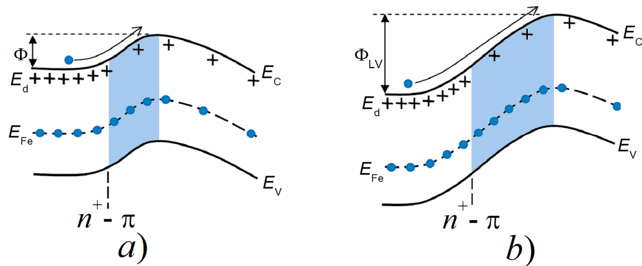

Fig. 5. (a) Schematic presentation of the band diagrams of n^+-π junction at LV = 0 and (b) LV < 0 (E_d - energy level of shallow donors, E_{Fe} - deep level of Fe acceptors, filled area corresponds to the negatively charged layer.

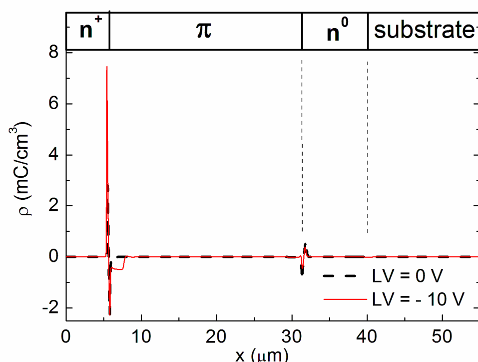

Fig. 6. Simulated profiles of space charge density for different bias of LV (at a time instant of t = 0 in Fig. 4b).

The average neutralization time for Fe traps is determined by the temperature (1) or the concentration of nonequilibrium holes (2). The expressions for these times can be written as follows [5]:

$$\tau_e = (\sigma_n v_n n_1)^{-1}, \quad (1)$$

$$\tau_c = (\sigma_p v_p p)^{-1}, \quad (2)$$

where τ_e and τ_c are the electron emission and hole capture time constants, v_n and v_p are the thermal velocities of electrons and holes, σ_n and σ_p are the electron and hole capture cross sections, p is the hole concentration, n_1 is the electron concentration when the Fermi level F is equal to Fe trap energy level.

For thermal emission of electrons, they need to overcome a barrier of at least 0.9 eV (E_g - ΔE_{Fe}), which significantly exceeds the ionization energy of iron ΔE_{Fe} = 0.5 eV. Moreover, the electron capture cross section is much smaller than the hole one [5, 9]. Hence, the most probable mechanism to neutralize traps is to capture holes from the valence band (2). However, even at the maximum concentrations of nonequilibrium holes near the n^+-π-junction (p = 10^{15} cm^{-3} [5]), the average capture time will be of about 1 μs (τ_c = $(\sigma_p \cdot v_p \cdot p)^{-1}$, where σ_p = 1.5·10^{-16} cm^2 and v_p = 10^7 cm/s). This capture time is much higher than the switching delay time that is of about tens of nanoseconds (Fig. 4). Therefore, the charged layer does not completely disappear when *S*-diodes operate in the pulse generation circuit. When *S*-diodes are being switched, the layer is static (superfast switching dynamics has nothing in common with trap recharging).

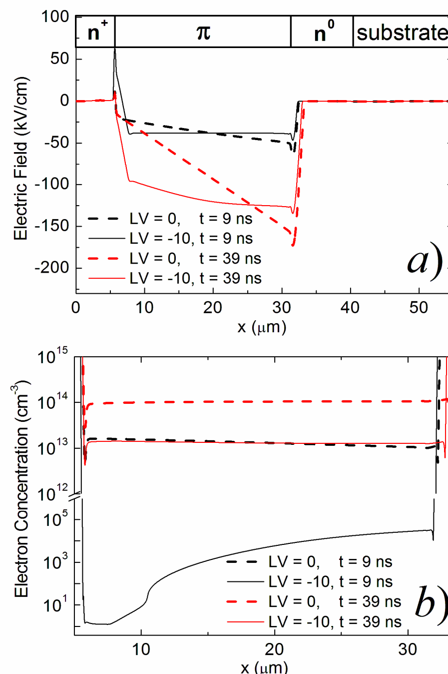

Fig. 7. (a) Simulated electric field profiles and (b) electron concentration profiles (for different bias of LV and time instants in Fig. 4b).

The AB circuit increases the *S*-diode switching voltage, since the lower the electron concentration in the π-layer, the higher the dynamic resistance (*dV(t)/dI(t)*) in the structure. The profiles of the electric field and electron concentration at different time instants are shown in Fig. 7. It can be seen that using the bias of LV = –10 V suppresses the injection from the n^+-π junction and increases the voltage supplied to the π-region (from a comparison of the electric field integrals for 39 ns). The calculations have shown an increase in the switching voltage of the avalanche *S*-diode from 250 to 334 V (in the experiment: from 238 to 294 V). This effect also improves the efficiency of the circuit, since the amplitude of the pulse current increases with increasing switching voltage [5].

CONCLUSION

The paper shows that dynamic current leakage in a pulsed power supply circuit based on an avalanche *S*-diode leads to significant charge losses at pulse durations of about 1 ns. In this case, the charge transferred to the load can be comparable to the leakage charge (several dozens of nC). The authors have shown that the use of an additional DC low-voltage bias with a polarity reversed to the high-voltage pulse reduces the pre-switching leakage by 3-4 times. Moreover, lesser leakage is attributed to a negatively charged layer of Fe traps near the electron injector (n^+-π-junction). The layer is disappearing for a relatively long time due to inert recharging of the traps. It increases the dynamic resistance of the *S*-diode before switching and increases the switching voltage by 20-30%. Lower leakage current can be expected to prevent the *S*-diode from overheating in the generator circuit and, as a consequence, to increase its reliability.

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