Broadband Analog Predistortion Circuits Utilizing Derivative Superposition

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***Abstract*—In this paper, we present two different broadband derivative superposition (DS) circuits for linearizing mmWave integrated circuits and small power amplifiers implemented using 22nm CMOS SOI technology. By combining two parallel devices with different biasing different nonlinear characteristics can be provided. Measured results showed more than 30 dB IM3 improvement for conventional DS circuit values by utilizing back-gate voltage on an auxiliary amplifier. Above 3 dB gain expansion was measured by a complementary DS circuit, which uses parallel NMOS and PMOS devices. This offers a simple analog predistortion circuit for an integrated small power amplifier, for example.**

Keywords—IMD, 1dB compression, back-gate biasing, 22nm FDSOI.

I. Introduction

Expanding worldwide digitalization has driven 3GPP to specify mmWave frequencies and wideband high PAPR signals (up to 400 MHz and 256-QAM OFDMA) for commercial use [1], which means that advanced node CMOS and SOI-CMOS processes are preferred for such high-frequency applications due to sufficient speed and compact size. However, the dynamic range is limited due to low supply voltages and challenging linearity requirements are calling for techniques to improve the linearity and increase the output swing of integrated power amplifiers. Stacked power amplifiers are often suggested [2] to increase the output swing but for all the remaining transceiver circuit blocks the available dynamic range is very limited. Another point of view is the efficiency vs. linearity, which the power amplifier is dominating by far. One would like to drive the PA closer to the saturation to maximize the efficiency, but average power is backed off from saturation around 6-10 dBs to meet the linearity requirements. For large phase arrays (proposed for 5G/6G mmWave transceivers [3]) where each antenna is driven by a small power PA, simple techniques are required to maximize the linearity and efficiency.

In this paper, we propose two derivative superposition circuits (DS) [4], [5], [6] to provide a means to minimize the distortion either by cancelling the IM3 of the amplification circuit itself or by providing predistortion characteristics for the following circuit such as compressive small PA. The proposed techniques are small and consume very little power. The idea is straightforward, by combining two parallel devices and bias them differently, we are able to generate IMD sweet spot (IMD of the devices are cancelling) or expansive characteristics (odd terms are summed up in-phase with the fundamental).

The organization of the paper is as follows: Section II reviews the operation of the proposed derivative superposition circuits, Section III shows the fabricated circuit and measurement setup. Measurement results are presented in Section IV and conclusions are drawn in Section V.

II. Circuit Design

A. Conventional Derivative Superposition

The conventional derivative superposition method uses two parallel NMOS transistors. The drain current of each transistor is presented in (1) and as they are summed up in a parallel transistor setup, it causes the following

$$i_{out} = i_{dm} + i_{da} = (g_{1m} + g_{1a})v_{gs} + (g_{2m} + g_{2a})v_{gs}^2 + (g_{3m} + g_{3a})v_{gs}^3 + \cdots, \quad (1)$$

where i_{dm} and i_{da} are drain currents of the main transistor and the auxiliary transistor, respectively. From here it can be seen that the small-signal transconductance coefficients (g_1, g_2, etc.) of different order are summed. Devices are biased so that g_{3m} and g_{3a} have opposite signs so that they cancel each other to reduce the IM3. To minimize the IM3, g_{3m} and g_{3a} have to be an exact opposite in phase and same in amplitude. At the same time, unfortunately, g_{2m} and g_{2a} have the same sign, causing high 2nd order intermodulation (which is a slight downside of the design).

In Figure 1, the schematic of the design is presented. Because both devices, M_1 and M_2 are dimensioned to be equal the input capacitances and resistances are the same. Both transistors are driven from the same input signal but use separate capacitors at the input side to isolate the different gate biases. The gate biases are created using individual DAC (Digital-to-Analog Converter) for each gate. The supply voltage (V_{DD}) is provided from the common output node. Usually, the V_{DD} is fed through a choke inductor to prevent the signal to leak to the DC supply, and the DC capacitor would be used to isolate the output from DC voltage. These parts were left out from the design as DC will be fed via

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external bias-tee during the measurements. What is also seen in Figure 1, is that back-gates (V_{bg1}, V_{bg2}) for the transistors M_1 and M_2 are enabled and for the auxiliary transistor, the back-gate will be utilized in the measurements. Back-gates of the transistors provide an alternate way of biasing the transistors [7].

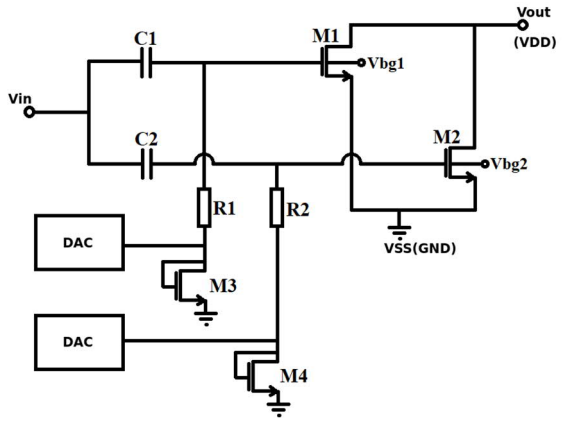

Figure 1. The schematic of the conventional derivative superposition circuit.

B. Complementary Derivative Superposition

Although, the conventional derivative superposition method is a good way to reduce the unwanted IM_3 it has its downsides. Because the 2nd order terms add up, the design is very sensitive to 2nd order nonlinearity. Complementary derivative superposition, using NMOS as well as PMOS (p-channel Metal-Oxide-Semiconductor) transistors, on the other hand, is capable of cancelling both even and odd-order distortion [6]. The output current of complementary derivative superposition is calculated as

$$i_{out} = i_{dn} - i_{dp} \tag{2}$$

and when the individual currents are examined, it can be seen why both even and odd-order terms are decreasing when biased correctly. Small-signal drain to source currents for NMOS and PMOS devices are as follows

$$i_{dn} = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \cdots \tag{3}$$

$$i_{dp} = -g_{1p} v_{gs} + g_{2p} v_{gs}^2 - g_{3n} v_{gs}^3 + \cdots. \tag{4}$$

From equations (3) and (4) it can be seen that the signs of odd terms are the opposite between the devices. When equations (3) and (4) are added to (2) we can write

$$i_{out} = (g_{1n} + g_{1p}) v_{gs} + (g_{2n} - g_{2p}) v_{gs}^2 + (g_{3n} + g_{3p}) v_{gs}^3 + \cdots, \tag{5}$$

where g_{1n}, g_{2n}, etc. are NMOS transistors coefficients and g_{1p}, g_{2p}, etc. are PMOS transistors coefficients. At first glance, it might seem that only the 2nd order terms are cancelling each other, but it happens also with 3rd order the same way it does in the conventional design. When the transistors are biased correctly the g_2 terms of both transistors have the same sign and at the same time, the g_3 terms have different signs. Hence, both terms are cancelling. However, there is a slight difference between optimal values for 2nd and 3rd order cancellation. Thus, depending on which is the desired quality, the optimization of gate biasing needs to be done.

Although for a complementary circuit there is room for adjustment between 2nd and 3rd order, neither of them were priorities when the circuit, in Figure 2, was designed. The conventional DS circuit (see Figure 1) was designed to minimize the IM3 of the circuit itself, while the complementary derivative superposition circuit was designed to provide gain expansion characteristics to act as a predistortion prior to the compressive small power amplifier. By using the complementary derivative superposition structure, it was possible to achieve expanding behaviour for the circuit and keeping it very simple.

In Figure 2 the transistor M_1 is a PMOS transistor, which is acting as an auxiliary device and the main device M_2 is an NMOS transistor. Input is driven, as in the other design, to both transistors and gates are biased by using DACs. The difference for this circuit is that the choke inductor L_1 was included in the on-chip circuit, as well as a DC capacitor C_3, both on the PMOS transistors source. A choke inductor is needed, to isolate the signal leaking to the V_{DD}. This affected the performance by not grounding the PMOS device in the small-signal model and could be fixed with a bypass capacitor to the ground. This allows the PMOS transistors source to be grounded from an alternating current (AC) perspective, but the supply voltage is still delivered to the circuit.

From the small-signal point of view, this causes the design to have LC parallel circuit at the source and, consequently, the resonance frequency may cause some issues at the circuit, if not dimensioned properly.

This complementary structure is a variation of a push-pull type amplifier and the expansive behaviour comes from the circuit biasing itself when more power is added to it. When more power is driven into the input of the amplifier, the voltage at the transistors shared drain, which is also used as the output node, rises. This causes the main transistor to conduct more which is seen as expansion in the gain.

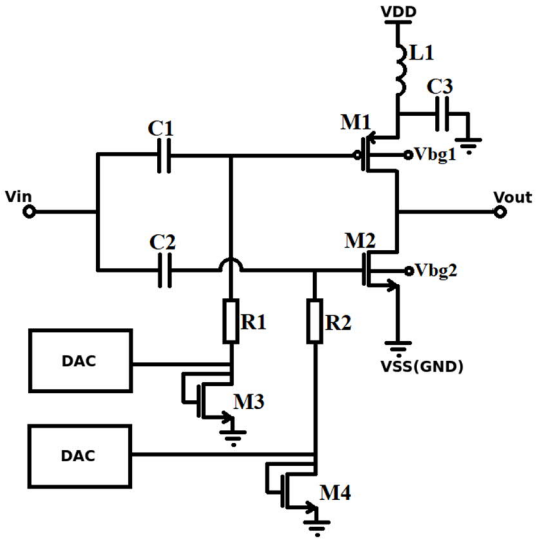

Figure 2. The schematic of the complementary derivative superposition circuit.

III. Implementation and Measurement Setup

The designs were implemented by using 22nm CMOS FDSOI technology suited for low-power IC designs [8]. The micrograph of the fabricated derivative superposition circuits is presented in Figure 3. Circuits were measured using on-chip probe measurements. Conventional derivative superposition circuit is the lower structure and higher is the complementary superposition circuit structure. In order to save the space in the chip, both circuits share one input and output ground pad in the middle of Figure 3. Additional size reduction was achieved by placing the choke inductor to the upper side of the design between the input and output probe pads, as is seen in Figure *3*. This way the width needed for the design between the pads was reduced from 54 µm (width of the inductor) to 13.4 µm. Complete dimensions of the design without and with the inductor, are 13.4 µm in width (W) and 34.4 µm in height (H) and 54 µm in width and 118.4 µm in height, respectively.

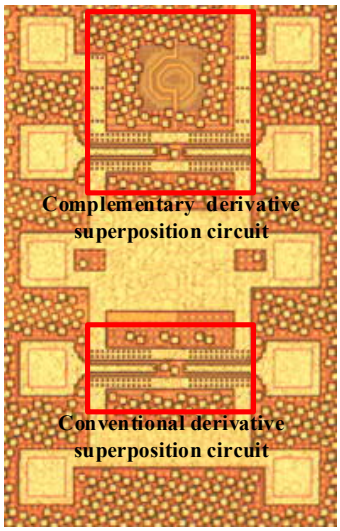

Figure 3. Micrograph of the manufactured derivative superposition circuits.

Because the conventional DS circuit has the output and the transistor drains at the same node, the same pad can be used to provide supply voltage and to measure the output signal. This is done with the off-chip bias-tee separating the line for the choke inductor and DC block capacitor. The conventional DS design somewhat determines the width of the whole design by being the wider circuit out of these two. The conventional design has a width of 22.9 µm and a height of 17.1 µm. The dimension of the whole combined design is 277.6 µm in width and 450 µm in height.

Keysight PNA-X 25 network analyser was used to measure the proposed circuits with Cascade Infinity I40 probes on a Cascade Microtech model 11000 probe station. A 2-tone test was used to measure the circuits. The proposed circuits were designed for 3GPP/NR FR2 frequency band, which includes frequencies from 24.5 GHz and above [1]. 2-tone measurement results were limited to center frequency of 25 GHz with 1 GHz tone spacing due to VNAs maximum frequency of 26.5 GHz. In addition, aliasing was observed at higher power levels. The power was calibrated at the end of the input cable. Then the measurement was normalized using a thru standard that was implemented on-chip. An automatic wideband power calibration (10 MHz – 26.5 GHz) was performed for 2-tone power sweep measurements. The actual input and output power were calculated by subtracting the measured losses of the probe and the thru.

IV. Measured Results

Frequency responses of both circuits are shown in Figure 4. The biasing for the conventional DS circuit is set to Vg1 = 650 mV and Vg2 = 150 mV for the main and auxiliary transistor, respectively. The threshold voltage for NMOS transistors is around 250 mV. For complementary DS circuit, the biasing is Vg1 = 190 mV and Vg2 = 630 mV for PMOS and NMOS devices, respectively. The threshold voltages are around 225 mV and 285 mV for the PMOS and the NMOS transistors, respectively. From the results we can see that the conventional DS is inherently wideband. Gain is decreasing less than 2 dB from 1 GHz to 26 GHz. On the other hand, complementary DS shows more variations, which is due to the implemented bias choke and AC grounding cap C3. The slope of the gain curves is more or less similar from 15 GHz onwards. The gain, in general, is low due to the fact that both circuits are measured from 50 ohm and there is no matching implemented i.e. there is an obvious mismatch. The lower and negative gain in complementary DS circuit is a combination of impedance mismatch, AC grounding and low gain in low input drive (prior to the expanding behaviour as shown in Figure *7*).

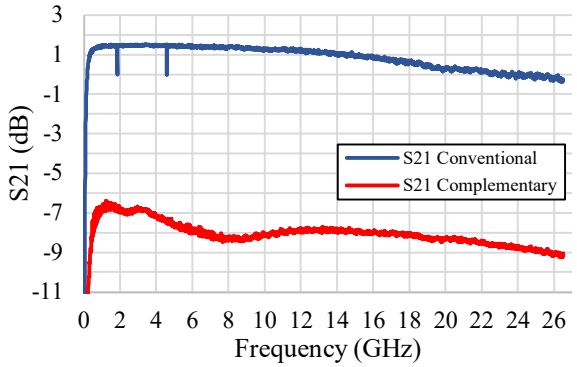

Figure 4. S21 of conventional and complementary DS circuits.

A. Conventional DS Circuit Measurements

Two-tone power sweep of conventional DS circuit at 25 GHz center frequency with 1 GHz tonespacing with different biasing schemes for the auxiliary transistor (M2 in Figure 1) is shown in Figure 5. The IM3 results are shown in dBc as a function of fundamental output power so that gain variation can be minimized and thus the results can be easily compared. When the auxiliary device is turned off (Vg2 = 0 V), high IM3 and low gain are observed. When the bias voltage is increased (green and red curves) to the auxiliary device IMD sweet spot is appearing at the Pout = -9 dBm and improvement in IM3 is more than 30 dB. In addition, the gain is increased due to the fact that the auxiliary device is also contributing to the total gain. Since 22nm CMOS SOI technology enables the use of back-gate biasing we set Vbg2 = 1.8 V (see gold curves in Figure 5.), which corresponds to around 135 mV of gate bias. We can see that IMD sweet spot appears at a lower output power level and remains low before the sweet spot (floor noise of the network analyser is affecting the measurement accuracy). In addition, the highest gain is

achieved with the use of back-gate biasing. This implies that the back-gate is a very useful way of biasing the auxiliary device for linearising purposes.

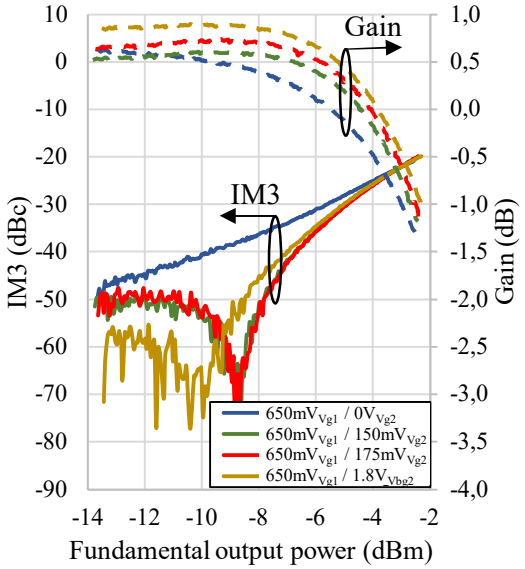

Figure 5. Conventional DS lower fundamental power gain and IM3 output power as a function of lower fundamental output power (f0 = 25 GHz, Tonespacing = 1 GHz).

In order to check the wideband behaviour of the conventional DS circuit, we performed two-tone measurements also at 15 GHz and 20 GHz center frequencies with 1 GHz tone spacing. The results with auxiliary device biased with Vbg2 = 1.5 V are shown in Figure 6. We can see that IM3 level remains below -50 dBc up to Pout = -10 dBm, which is very low in terms of dBc in every frequency, 15 GHz curve being slightly lower than others. Altogether, IMD cancellation using a parallel auxiliary transistor with correct biasing provides an excellent and easy means to provide wideband linearization for various integrated circuit structures.

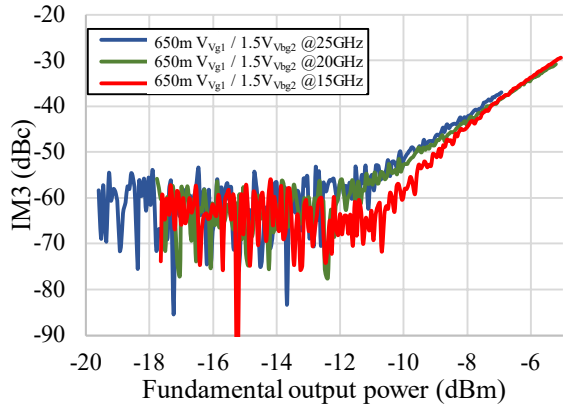

Figure 6. Conventional DS lower IM3 output power as a function of lower fundamental output power with different center frequencies (tonespacing 1 GHz).

B. Measurements of Complementary DS Circuit

With a conventional DS circuit, the purpose was to linearize the circuit itself in terms of cancelling the IM3 of the main transistor by biasing the auxiliary transistor the way that the phases of the IM3 are the opposite as explained in Section II.A. Complementary DS circuit is able to provide similar cancellation but the aim here was to provide a gain expanding behaviour so that it can linearise e.g. integrated power amplifier that is operating close to compression point for providing better efficiency. Here the aim is to be able to tune the level of gain and expansion (see Figure 7) so that we are able to match the expanding curve to the compressive curve of the PA. Note that the peak to average power ratio (PAPR) of modern modulated signals can be above 10 dB, thus the operating range in terms of a power sweep of the expanding predistorter needs also be around 10 dB. In addition, it should be noted that the saturation power of the PA is often very close to 3dB compression point and thus expansion around 3 dB is sufficient.

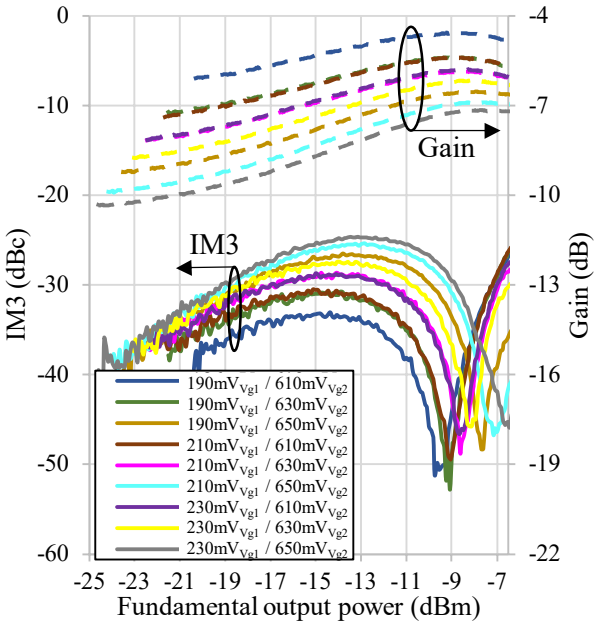

Figure 7. Complementary DS lower fundamental gain (dB) and IM3 (dBc) as a function of lower fundamental output power (dBm) (f0 = 25 GHz, tonespacing = 1 GHz).

The performance of the circuit with different biasing points is represented in Figure 7. The gain and IM3 were measured with three different gate voltages for both transistors (9 different biasing cases in total). Expansive gain characteristics are obvious and with biasing we can control the level of the gain and also expansive characteristics. Depending on the biases, the low power gain is changing for over 4 dB and it is capable of an even wider range of variation as the gate voltages for both transistors only change circa 40 mV over the three gate biases. The expansion in the circuit is caused by the positive 3rd order nonlinearity term, which causes the gain of the circuit to expand until the point where the term rotates and starts to compress the signal. With the lower gain, the 3rd order term is affecting the gain more heavily causing the circuit to achieve around 3 dB of expansion. As the circuit is biased to have more gain, the impact of the 3rd order term diminishes and the expansion is more minor. This kind of behaviour allows the circuit to be adjustable to fit several types of PAs. Depending on the compression and desired qualities of the amplifier, the predistorter can be adjusted accordingly. What comes to the IM3 performance of the circuit, the dBc value is relatively high. This is due to the fact that the circuit is a highly nonlinear, but purposely opposite character to the compressive PA. The results indicate that as the expansion is

lower (and the gain is higher) the circuit generates lower IM3 compared to the fundamental than with higher expansion. There is also an IM3 sweet spot generated which is somewhat dependent on the compression of the circuit. With the lower expansion, the circuit starts to compress earlier, causing the sweet spot to occur earlier.

The frequency dependency of the expansive behaviour is presented in Figure 8 and Figure 9, from where we can see that the expansive characteristics are similar regardless of the frequency. The maximum gain is varying less than 1.5 dB from 15 GHz to 25 GHz, while the IM3 curves in terms of dBc are very similar, showing very small frequency-dependent variation regardless of the fact that the circuit contains bias choke, AC-grounding cap and DC block. The effect of the tonepacing at 25 GHz is shown in Figure 9. It can be seen that gain is 1.5 dB higher at tonespacing of 10 MHz, but gain curves are nicely overlapping with 100 MHz and 1 GHz tonespacing. IM3 curves are similar in dBc values, but the IMD sweet spot is occurring at higher output power when tonespacing is increased. These variations imply some frequency dependency, probably related to memory effects.

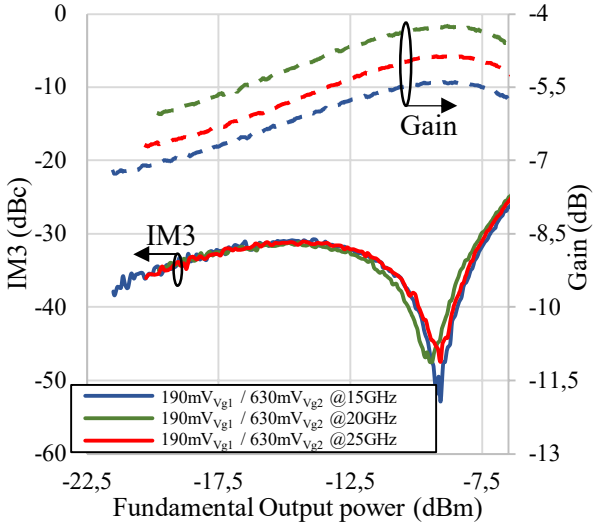

Figure 8. Complementary DS lower fundamental gain and IM3 output power as a function of lower fundamental output power (tonespacing = 1 GHz).

V. Conclusions

In this paper, we proposed derivative superposition circuits for linearizing the mmWave integrated circuits. Conventional DS circuit combines two parallel NMOS devices that are biased separately to minimize the IM3, while in complementary DS circuit NMOS and PMOS devices are connected to provide expansive gain characteristics. With proper biasing conventional DS circuit is able to generate IMD sweet spot where IM3 is improved over 30 dB. With the use of a back-gate for the auxiliary device the smallest IM3 and highest gain were measured. The complementary DC circuit was biased to provide above 3 dB gain expansion. The level of gain and shape of expansion is controllable via gate biasing. Both circuits were observed to be broadband from 15 GHz to 25 GHz frequency range being suitable linearization purposes for mmWave integrated circuits.

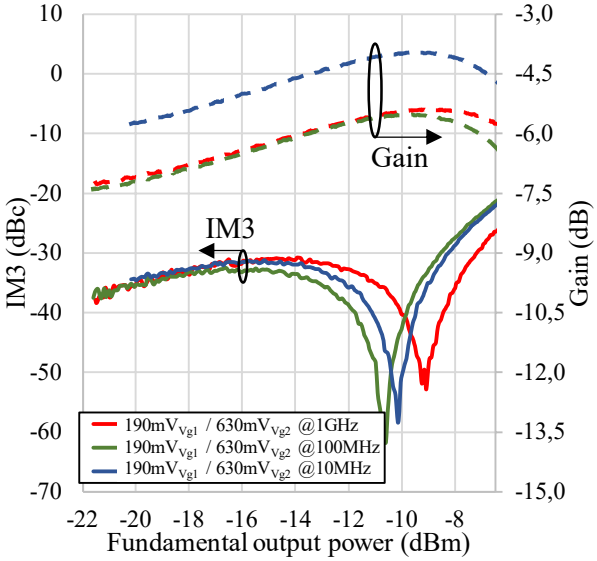

Figure 9. Complementary DS lower fundamental gain and IM3 output power as a function of lower fundamental output power with different tone widths (f0 = 25 GHz).

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